User's Manual

ASSP

R-IN32M3 Series User's Manual

- R-IN32M3-EC

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Instructions for the use of product

In this section, the precautions are described for over whole of CMOS device.
Please refer to this manual about individual precaution.
When there is a mention unlike the text of this manual, a mention of the text takes first priority

1.Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

-The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2.Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

-The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3.Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

-The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4.Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

-When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

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・Real-Time OS　Accelerator and Hardware Real-Time OS is based on Hardware Real-Time OS of “ARTESSO” made in KERNELON SILICON Inc.

How to use this manual

1. Purpose and target readers

This manual is intended for users who wish to understand the functions of Industrial Ethernet network LSI "R-IN32M3-EC" (MC-10287F1-HN4-A) for designing application of it.

It is assumed that the reader of this manual has general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

Literature — Literature may be preliminary versions. Note, however, that the following descriptions do not indicate "Preliminary". Some documents on cores were created when they were planned or still under development. So, they may be directed to specific customers. Last four digits of document number(described as ****) indicate version information of each document. Please download the latest document from our web site and refer to it.

The document related to R-IN32M3-EC

Document name	Document number
R-IN32M3 series Datasheet	R18DS0008EJ****
R-IN32M3-CL User's Manual	R18UZ0005EJ****
R-IN32M3 series User's Manual Peripheral function	R18UZ0007EJ****
R-IN32M3 Series Proguraming Manual (OS edition)	R18UZ0011EJ****
R-IN32M3 Series Proguraming Manual (Driver edition)	R18UZ0009EJ****
R-IN32M3-EC User's Manual	This manual

2. Notation of Numbers and Symbols

Weight in data notation: Left is high-order column, right is low-order column

Active low notation:

xxxZ (capital letter Z after pin name or signal name)

or xxx_N (capital letter _N after pin name or signal name)

or xxnx (pin name or signal name contains small letter n)

Note:

explanation of (Note) in the text

Caution:

Item deserving extra attention

Remark:

Supplementary explanation to the text

Numeric notation:

Binary ⋯ xxxx , xxxxB or n'bxxxx (n bits)

Decimal ⋯ xxxx

Hexadecimal ⋯ xxxxH or n'hxxxx (n bits)

Prefixes representing powers of 2 (address space, memory capacity):

K (kilo)⋯ $2^{10} = 1024$

M (mega)⋯ $2^{20} = 1024^2$

G (giga)⋯ $2^{30} = 1024^3$

Data Type:

Word ⋯ 32 bits

Halfword ⋯ 16 bits

Byte ⋯ 8 bits

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1. Overview

1.1 Introduction

Ethernet communication continues to spread rapidly in the field of industrial automation as manufacturers seek to improve the capability, efficiency, and flexibility of their organizations. Modern Industrial Ethernet applications require high-speed real-time response, low power consumption, and high performance. These requirements are not necessarily met by traditional methods such as hard-wired Ethernet processors or dedicated high-speed CPUs.

Renesas' R-IN32M3-EC of large-scale integrated circuits (LSI) are specifically tailored to meet the demands of Industrial Ethernet applications. Key features include:

- High-speed, real-time, deterministic, low-latency, low-jitter response for real-time applications
- Low power consumption
- Integrated ARM Cortex-M3 core for flexibility
- Integrated Real-Time OS Accelerator with support for µITRON version 4.0
- Integrated 10/100Mbps EtherPHY
- Dedicated, DMA controller and buffer for the network processor
- High performance with low CPU usage by offloading functions to Real-Time OS Accelerator
- Multiple timers, serial interfaces, general purpose I/O (GPIO), external memory interfaces

1.2 Overview

Table 1.1 Overview of R-IN32M3-EC(1/2)

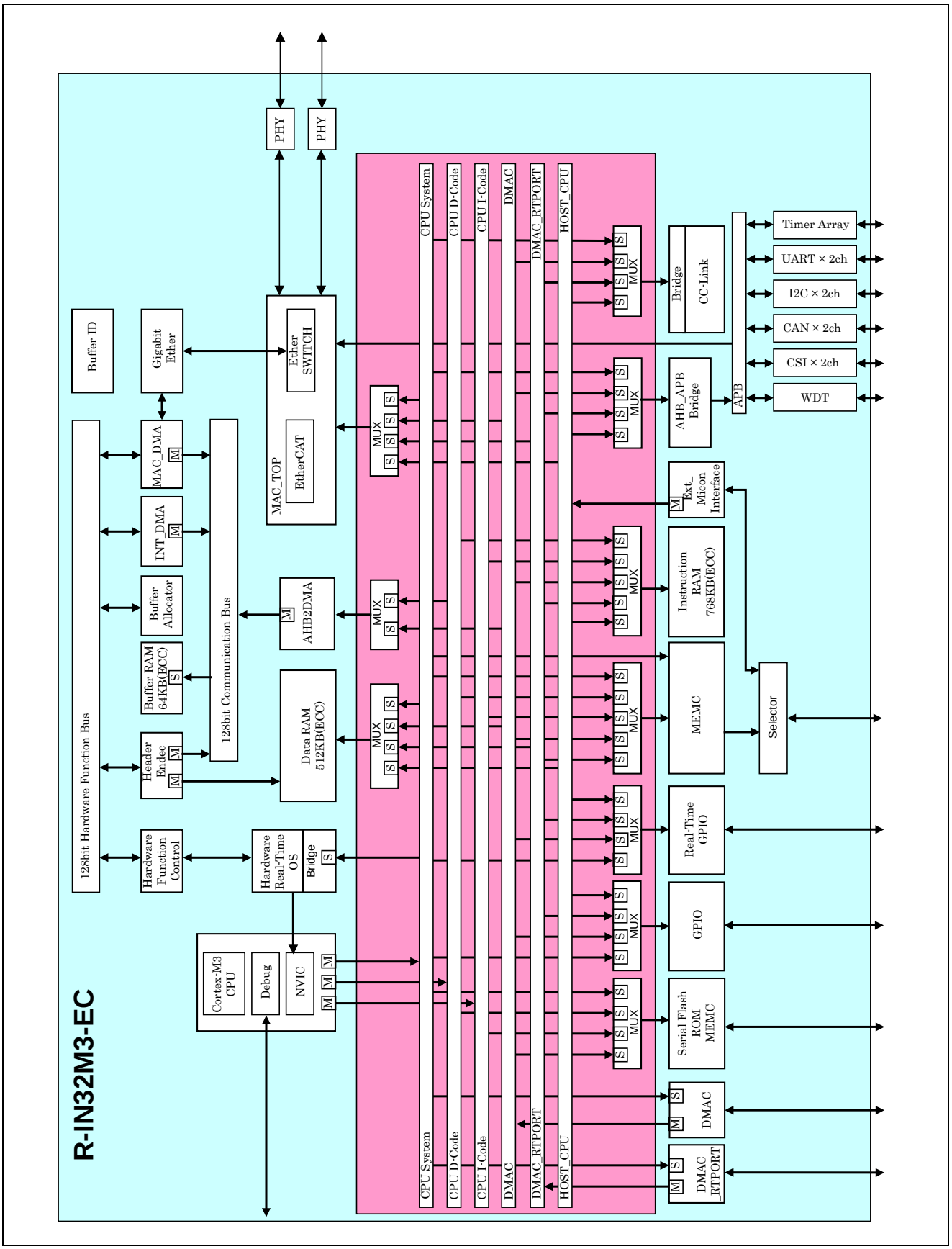
Item \ Product	R-IN32M3-EC
CPU core	ARM Cortex-M3 32-bit RISC CPU + Real-Time OS Accelerator (Hardware Real-Time OS, HW-RTOS)
Operating frequency	100MHz
Instruction set	Thumb®-2 instruction ARMv7-M architecture
Instruction RAM	768KByte (RAM w/ECC)
Data RAM	512KByte (RAM w/ECC)
Buffer RAM	64KByte (RAM w/ECC)
Internal System Bus	- 32-bit system bus at 100MHz - 128-bit communication bus at 100MHz
DMA Bus (System Bus Side)	- 4 channels + 1 channel (for Real-time port) - Supports software and various interrupt-triggered DMA
Boot options	- Serial Flash ROM Boot - External Memory Boot - External MPU Boot
External Memory Support	- 16-bit or 32-bit bus interface - Page ROM / ROM / SRAM interface - Synchronous burst memory interface - Four chip selects for external SRAM - 256MByte (max) external memory space - Programmable wait function
External MPU interface	- 16-bit or 32-bit bus interface - General-purpose interface for static memory - Address space:2MByte (Instruction RAM, Data RAM, Register area)
Serial Flash ROM Memory Controller	- Support serial interface compatible with SPI of the companies - Support direct boot from serial memory device - Support Fast Read, Fast Read Dual Output, Fast Read Dual I/O mode - Direct layout in memory space
Interrupt Support	- 29 external interrupt ports
Internal Peripherals	
I/O Ports	CMOS I/O:96ports(max)
System Timers	- Internal timer of Hardware RTOS
	- internal timer of CPU
	- 4channel timer array - 32bit counter & 32bit data register - counter by external signal

Table 1.1 Overview of R-IN32M3-EC(2/2)

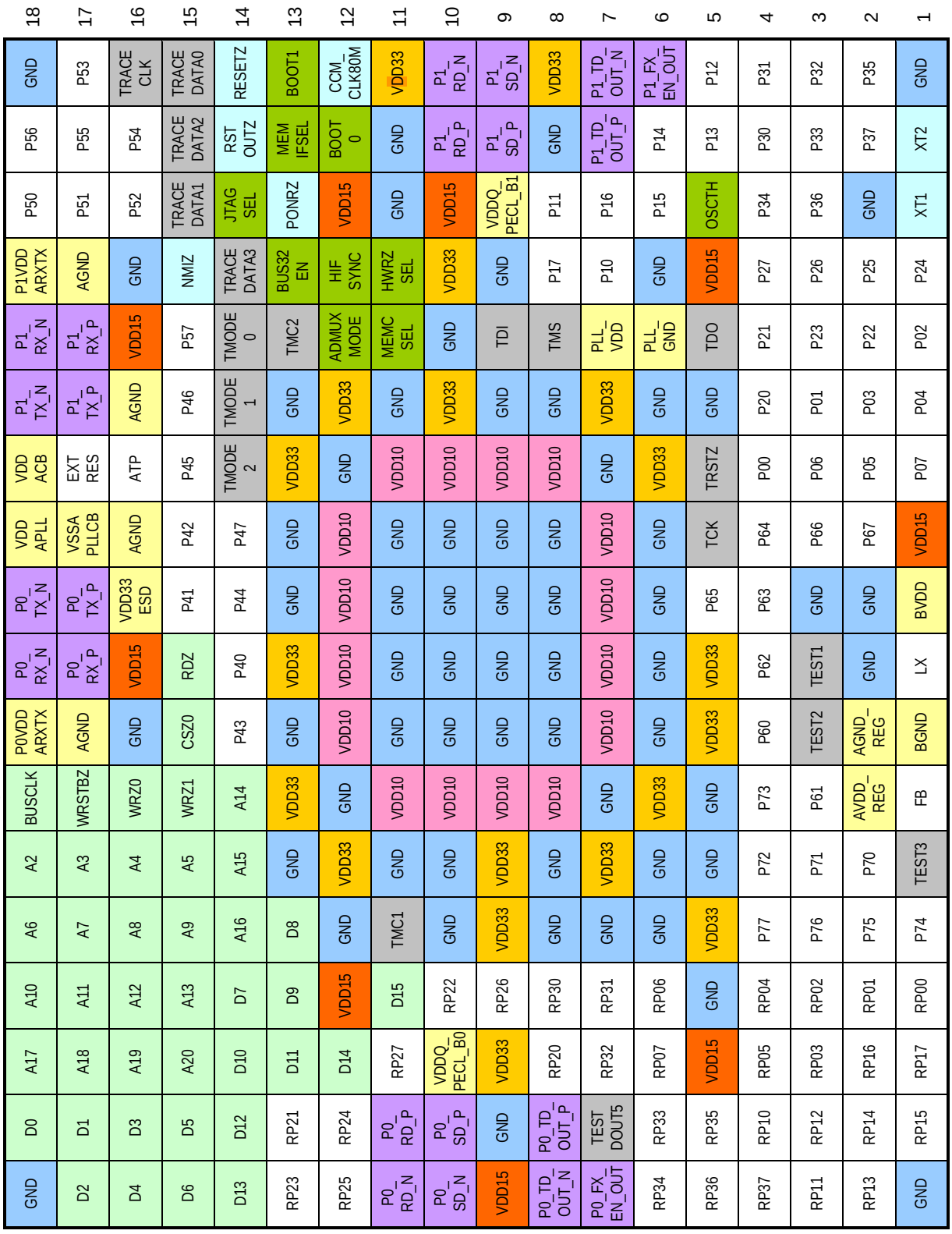
Item \ Product	R-IN32M3-EC
Internal Peripherals (cont.)	
Watchdog Timer	- 1 channel - Software-triggered start mode - Watchdog error response options: - Generate Non-Maskable Interrupt (NMI) - Generate Reset
Asynchronous serial interface	- 2 channels - Full duplex - FIFOs: 10-bit x 16 receive and 8-bit x 16 transmit - Support output of receive errors and status - Character length: 7 or 8-bit - Parity bit options: odd, even, 0- , none - Transmit stop bits: 1 or 2-bit
I2C Serial interface	- 2 channels - Operation modes: normal or high-speed - Transfer modes: single-transfer mode, or continuous-transfer mode - Transmission data length: 8-bit
CAN controller	- 2 channels - Conforming to ISO11898 - Support to transfer and receive normal frame and expand frame - Transmission speed: 1Mbps (max)
Clock Synchronized Serial Interface	- 2 channels - Synchronized Serial data transmission by three-wire system - Selectable Master mode or Slave mode - Built-in Baud-rate generator - Transmission data length: 7bit - 16bit
CC-Link	- Intelligent device station Note3 <R> - Remote device station
10/100Mbps EtherPHY Note2	- 2ports - Support for 10BaseT and 100BaseTX/FX
EtherCAT	EtherCAT Slave controller
On-chip debug function	- Select serial wire or JTAG - Support Full Trace (Built-in ETM)
Internal PLL	Generates various clocks from 25MHz input clock
Power supply voltage	I/O:VDD33 = 3.3±0.3V Internal circuit :VDD10 = 1.0±0.1V

Note. Please ask us about a detail for support.

1.3 INTERNAL BLOCK DIAGRAM



1.4 Pin Placement (Top View)



	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
A	GND	D2	D4	D6	D13	RP23	RP25	P0_RD_N	P0_SD_N	VDD15	P0_TD_OUT_N	P0_FX_EN_OUT	RP34	RP36	RP37	RP11	RP13	GND
B	D0	D1	D3	D5	D12	RP21	RP24	P0_RD_P	P0_SD_P	GND	P0_TD_OUT_P	TEST DOUT5	RP33	RP35	RP10	RP12	RP14	RP15
C	A17	A18	A19	A20	D10	D11	D14	RP27	VDDQ_PECL_B0	VDD33	RP20	RP32	RP07	VDD15	RP05	RP03	RP16	RP17
D	A10	A11	A12	A13	D7	D9	VDD15	D15	RP22	RP26	RP30	RP31	RP06	GND	RP04	RP02	RP01	RP00
E	A6	A7	A8	A9	A16	D8	GND	TMC1	GND	VDD33	GND	GND	GND	VDD33	P77	P76	P75	P74
F	A2	A3	A4	A5	A15	GND	VDD33	GND	GND	VDD33	GND	VDD33	GND	GND	P72	P71	P70	TEST3
G	BUSCLK	WRSTBZ	WRZ0	WRZ1	A14	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	GND	P73	P61	AVDD_REG	FB
H	P0VDD ARXTX	AGND	GND	CS20	P43	GND	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	P60	TEST2	AGND_REG	BGND
J	P0_RX_N	P0_RX_P	VDD15	RDZ	P40	VDD33	VDD10	GND	GND	GND	GND	VDD10	GND	VDD33	P62	TEST1	GND	LX
K	P0_TX_N	P0_TX_P	VDD33 ESD	P41	P44	GND	VDD10	GND	GND	GND	GND	VDD10	GND	P65	P63	GND	GND	BVDD
L	VDD APLL	VSSA PLLCB	AGND	P42	P47	GND	VDD10	GND	GND	GND	GND	VDD10	GND	TCK	P64	P66	P67	VDD15
M	VDD ACB	EXT RES	ATP	P45	TMODE 2	VDD33	GND	VDD10	VDD10	VDD10	VDD10	GND	VDD33	TRSTZ	P00	P06	P05	P07
N	P1_TX_N	P1_TX_P	AGND	P46	TMODE 1	GND	VDD33	GND	VDD33	GND	GND	VDD33	GND	GND	P20	P01	P03	P04
P	P1_RX_N	P1_RX_P	VDD15	P57	TMODE 0	TMC2	ADMUX MODE	MEMC SEL	GND	TDI	TMS	PLL_VDD	PLL_GND	TDO	P21	P23	P22	P02
R	P1VDD ARXTX	AGND	GND	NMIZ	TRACE DATA3	BUS32 EN	HIF SYNC	HWRZ SEL	VDD33	GND	P17	P10	GND	VDD15	P27	P26	P25	P24
T	P50	P51	P52	TRACE DATA1	JTAG SEL	PONRZ	VDD15	GND	VDD15	VDDQ_PECL_B1	P11	P16	P15	OSCTH	P34	P36	GND	XT1
U	P56	P55	P54	TRACE DATA2	RST OUTZ	MEM IFSEL	BOOT 0	GND	P1_RD_P	P1_SD_P	GND	P1_TD_OUT_P	P14	P13	P30	P33	P37	XT2
V	GND	P53	TRACE CLK	TRACE DATA0	RESETZ	BOOT1	CCM_CLK80M	VDD33	P1_RD_N	P1_SD_N	VDD33	P1_TD_OUT_N	P1_FX_EN_OUT	P12	P31	P32	P35	GND
	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V

2. Signals by function

2.1 Signals by function

2.1.1 Ethernet Signal

(1) Media Interface

Pin Name	I/O	Function	Active	Level during reset & Level after reset
P0_RX_P	I	PHY0 Receive data (+)	-	-
P0_RX_N	I	PHY0 Receive data (-)	-	-
P1_RX_P	I	PHY1 Receive data (+)	-	-
P1_RX_N	I	PHY1 Receive data (-)	-	-
P0_TX_P	O	PHY0 Transmit data (+)	-	-
P0_TX_N	O	PHY0 Transmit data (-)	-	-
P1_TX_P	O	PHY1 Transmit data (+)	-	-
P1_TX_N	O	PHY1 Transmit data (-)	-	-
P0_SD_P	I	PHY0 100BASE-FX Signal Detect (+)	High	-
P0_SD_N	I	PHY0 100BASE-FX Signal Detect (-)	Low	-
P1_SD_P	I	PHY1 100BASE-FX Signal Detect (+)	High	-
P1_SD_N	I	PHY1 100BASE-FX Signal Detect (-)	Low	-
P0_RD_P	I	PHY0 100BASE-FX Receive data (+)	-	-
P0_RD_N	I	PHY0 100BASE-FX Receive data (-)	-	-
P1_RD_P	I	PHY1 100BASE-FX Receive data (+)	-	-
P1_RD_N	I	PHY1 100BASE-FX Receive data (-)	-	-
P0_TD_OUT_P	O	PHY0 100BASE-FX Transmit data (+)	-	-
P0_TD_OUT_N	O	PHY0 100BASE-FX Transmit data (-)	-	-
P1_TD_OUT_P	O	PHY1 100BASE-FX Transmit data (+)	-	-
P1_TD_OUT_N	O	PHY1 100BASE-FX Transmit data (-)	-	-
P0_FX_EN_OUT	O	PHY0 100BASE-FX FX Enable Indication 1：100BASE-FX mode	High	-
P1_FX_EN_OUT	O	PHY1 100BASE-FX FX Enable Indication 1：100BASE-FX mode	High	-

Remark In MDI-X mode, the input and output attributes of TXP/TXN and RXP/RXN are reversed.

(2) Other Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
P0LINKLEDZ	O	SIP_PHY0 Link status LED port	P06	Low	Hi-Z
P1LINKLEDZ	O	SIP_PHY1 Link status LED port	P07	Low	
ETHSWSECOUT	O	EtherSwitch Event par 1sec output port	P24	High	Hi-Z With internal pull-up resistor
P0DUPLEXLEDZ	O	SIP_PHY0 half-duplex status LED port Note2 0 : full-duplex 1 : half-duplex	P70	-	
P0SPEED100LEDZ	O	SIP_PHY0 100-BASE status LED port Note2	P72	Low	
P0SPEED10LEDZ	O	SIP_PHY0 10-BASE status LED port Note2	P73	Low	
P1DUPLEXLEDZ	O	SIP_PHY1 half-duplex status LED port Note2 0 : full-duplex 1 : half-duplex	P74	-	
P1SPEED100LEDZ	O	SIP_PHY1 100-BASE status LED port Note2	P76	Low	
P1SPEED10LEDZ	O	SIP_PHY1 10-BASE status LED port Note2	P77	Low	
P0ACTLEDZ	O	SIP_PHY0 RX status LED port Note2	RP02	Low	
P1ACTLEDZ	O	SIP_PHY1 TX status LED port Note2	RP04	Low	

2.1.2 EtherCAT Slave Controller Signal

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CATLEDRUN	O	Ether CAT RUN LED port	P00	High	Hi-Z
CATIRQ	O	Ether CAT IRQ port	P01	High	
CATLEDSTER	O	Ether CAT Dual-color State LED port	P02	High	
CATLEDERR	O	Ether CAT Error LED port	P03	High	
CATLINKACT0, CATLINKACT1	O	Ether CAT Link / Activity LED port	P04-P05	High	
CATSYNC1	O	Ether CAT SYNC1 port	P10	High	Hi-Z With internal pull-up resistor
CATSYNC0	O	Ether CAT SYNC0 port	P11	High	Hi-Z With internal pull-down resistor
CATLATCH1	I	Ether CAT LATCH1 port	P10	High	Hi-Z With internal pull-up resistor
CATLATCH0	I	Ether CAT LATCH0 port	P11	High	Hi-Z With internal pull-down resistor
CATI2CCLK	O	Ether CAT EEPROM I2C clock port	P22	-	Hi-Z
CATI2CDATA	I/O	Ether CAT EEPROM I2C data port	P23	-	
CATRESTOUT	O	Ether CAT PHY RESETOUT port	P56	-	Hi-Z With internal pull-up resistor

2.1.3 External Memory Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset	Level after reset
BUSCLK	O	Bus clock output port	-	-	-	-	-
CSZ0	O	Chip select signal output port	HCSZ	-	Low	Hi-Z With internal pull-up resistor	High
CSZ1	O		HPGCSZ	P44			Hi-Z With internal pull-up resistor
CSZ2	O		-	P51			
CSZ3	O		-	P50			
A1	O	Address output port	HA1	P40	-	Hi-Z With internal pull-up resistor	Low
A2-A20	O		HA2-HA20	-		Hi-Z With internal pull-down resistor	
A21-A27	O		-	RP21-RP27			Hi-Z With internal pull-down resistor
D0-D15 Note1	I/O	Data bus port	HD0-HD15	-			
D16-D31 Note1	I/O		HD16-HD31	RP30-RP37 RP10-RP17	-	Hi-Z With internal pull-up resistor	
RDZ	O	Read strobe output port	HRDZ	-	Low	Hi-Z With internal pull-up resistor	High
WRSTBZ	O	Write strobe output port	HWRSTBZ	-	Low		
WRZ0, WRZ1/ BENZ0, BENZ1	O	Effectively Byte lane strobe output port	HWRZ0, HWRZ1/ HBENZ0, HBENZ1	-	Low		
WRZ2, WRZ3/ BENZ2, BENZ3	O		HWRZ2, HWRZ3/ HBENZ2, HBENZ3	RP06, RP07			
WAITZ	I	Wait signal input port	HWAITZ	P41	Low	Hi-Z With internal pull-up resistor	
WAITZ1-WAITZ3 Note2			-	P45-P47			
BCYSTZ / ADVZ Note3	O	Address valid output port	HBCYSTZ	RP20	Low	Hi-Z With internal pull-up resistor	

Remark External Memory Interface Signal expects BUSCLK is an input signal while the internal reset signal (HRESETZ) is active.

Note1. When using synchronous burst access MEMC this port is shared with Address port when ADMUXMODE is high.

Note2. This port is available only when using synchronous burst access MEMC.

Note3. This port functions as BCYSTZ when using asynchronous SRAM MEMC, it functions as ADVZ when using synchronous burst access MEMC

2.1.4 External MPU Interface Signals

Pin Name	I/O	Function	Shared Signal	Shared port	Active	Level during reset & Level after reset
HBUSCLK	I	Bus clock for Host MPU output port	INTPZ11	P43	-	Hi-Z With internal pull-up resistor
HCSZ	I	Chip select signal input port	CSZ0	-	Low	
HPGCSZ	I	Pogrom mode Chip select signal input port	CSZ1	P44	Low	
HWAITZ	O	Wait signal output port	WAITZ	P41	Low	
HA1	I	Address input port	A1	P40	-	Hi-Z With internal pull-up resistor
HA2-HA20	I		A2-A20	-		Hi-Z With internal pull-down resistor
HD0-HD15	I/O	Data bus port	D0-D15	-	-	
HD16-HD31	I/O		D16-D31	RP30-RP37 RP10-RP17		Hi-Z With internal pull-up resistor
HRDZ	I	Read strobe input port	RDZ	-	Low	Hi-Z With internal pull-up resistor
HWRSTBZ	I	Write strobe output port	WRSTBZ	-	Low	
HWRZ0, HWRZ1/ HBENZ0,HBENZ1	I	Effectively Byte lane strobe input port	WRZ0, WRZ1/ BENZ0, BENZ1	-	Low	
HWRZ2, HWRZ3/ HBENZ2,HBENZ3	I		WRZ2, WRZ3/ BENZ2, BENZ3	RP06, RP07		
HERROUTZ	O	Error interrupt output port	SLEEPING	P42	Low	High
HBCYSTZ	I	Bus cycle input port	BCYSTZ / ADVZ	RP20	Low	Hi-Z With internal pull-up resistor

Caution When you use asynchronous mode, please input Low into a HBUSCLK pin..

Remark External MPU interface signals operate as an External MPU interface durinug reset.

2.1.5 Port Signals, Real-time port Signals

Port Signals and Real-time port Signals are configured as 12 sets of 8-bit ports.
They are able to realize 32-bit access by grouping 4 ports; i.e. Ports 0-3, Ports 4-7 or Real-time ports 0-3.

(1/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P0	P00	INTPZ0	CATLEDRUN	-	-	Hi-Z
	P01	INTPZ1	CATIRQ	-	-	
	P02	INTPZ2	CATLEDSTER	-	-	
	P03	INTPZ3	CATLEDERR	-	CCS_MON5	
	P04	INTPZ4	CATLINKACT0	-	CCS_MON6	
	P05	INTPZ5	CATLINKACT1	-	CCS_MON7	
	P06	-	P0LINKLEDZ	-	CCS_MON0	
	P07	-	P1LINKLEDZ	-	CCS_RESOUT	
P1	P10	CATLATCH1	CATSYNC1	-	CCS_REFSTB	Hi-Z With internal pull-up resistor
	P11	CATLATCH0	CATSYNC0	-	CCS_MON4	Hi-Z With internal pull-down resistor
	P12	INTPZ6	-	-	-	Hi-Z With internal pull-up resistor
	P13	INTPZ7	-	CCS_WDTZ / CCM_WDTENZ	-	
	P14	SMSCK	-	-	-	
	P15	SMSI	-	-	-	
	P16	SMSO	-	-	-	
	P17	SMCSZ	-	-	-	
P2	P20	RXD0	−	CCM_LINKERRZ	-	Hi-Z
	P21	TXD0	−	CCM_ERRZ	-	
	P22	INTPZ8	CATI2CCLK	CCS_IOTENSU	-	
	P23	INTPZ9	CATI2CDATA	CCS_SENYU0	-	
	P24	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-	
	P25	WDTOUTZ	−	CCS_ERRZ	-	
	P26	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-	
	P27	TIN0	TOUT0	-	-	

(2/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P3	P30	RXD1	-	-	-	Hi-Z With internal pull-up resistor
	P31	TXD1	-	-	-	
	P32	DMAREQZ1	-	-	CCS_MON1	
	P33	DMAACKZ1	-	-	CCS_MON2	
	P34	DMATCZ1	-	-	CCS_MON3	
	P35	CSISCK1	INTPZ22	CCM_IRLZ	-	
	P36	CSISI1	INTPZ23	CCS_FUSEZ	-	
	P37	CSISO1	INTPZ24	CCM_MSTZ	-	
P4	P40	A1	HA1	-	-	Hi-Z With internal pull-up resistor
	P41	WAITZ	HWAITZ	-	-	
	P42	SLEEPING	HERROUTZ	CCM_SDGCZ	-	
	P43	INTPZ11	HBUSCLK	-	-	
	P44	CSZ1	HPGCSZ	-	-	
	P45	CSISCK0	WAITZ1	-	-	
	P46	CSISI0	WAITZ2	-	-	
	P47	CSISO0	WAITZ3	-	-	
P5	P50	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-	
	P51	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-	
	P52	TIN3	TOUT3	CCS_SDGATEON	-	Hi-Z With internal pull-down resistor
	P53	CRXD0	CCS_RD	CCM_RD	-	Hi-Z With internal pull-up resistor
	P54	CTXD0	CCS_SD	CCM_SD	-	
	P55	CRXD1	-	-	-	
	P56	CTXD1	CATRESTOUT	-	-	
	P57	TIN2	TOUT2	-	-	

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	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
P6	P60	SCL0	−	−	−	Hi-Z
	P61	SDA0	−	−	−	
	P62	RTDMAREQZ	−	CCM_MDIN0	−	
	P63	RTDMAACKZ	−	CCM_MDIN1	−	
	P64	RTDMATCZ	−	CCM_MDIN2	−	
	P65	DMAREQZ0	−	CCM_MDIN3	−	
	P66	DMAACKZ0	−	-	−	
	P67	DMATCZ0	−	−	−	
P7	P70	CSICS00	P0DUPLEXLEDZ	CCS_STATION_NO_0 / CCM_SNIN0	−	
	P71	CSICS01	−	CCS_STATION_NO_1 / CCM_SNIN1	−	
	P72	CSICS10	P0SPEED100LEDZ	CCS_STATION_NO_2 / CCM_SNIN2	−	
	P73	CSICS11	P0SPEED10LED	CCS_STATION_NO_3 / CCM_SNIN3	−	
	P74	INTPZ12	P1DUPLEXLEDZ	CCS_STATION_NO_4 / CCM_SNIN4	−	
	P75	INTPZ13	−	CCS_STATION_NO_5 / CCM_SNIN5	−	
	P76	INTPZ14	P1SPEED100LEDZ	CCS_STATION_NO_6 / CCM_SNIN6	−	
	P77	INTPZ15	P1SPEED10LEDZ	CCS_STATION_NO_7 / CCM_SNIN7	−	

RP0x-RP3x are Real-time ports which can transfer data via a dedicated DMA comtroller, and are unaffected by bus congestion. They are able to perform input and output of the port by 32 bit unit in sync with DMA transfer trigger by DMA Controller for exclusive use of the Real-time port..

(4/4)

	Port Name	Mode 1	Mode 2	Mode 3	Mode 4	Level during reset & Level after reset
RP0	RP00	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	−	Hi-Z With internal pull-up resistor
	RP01	INTPZ17	SDA1	CCM_SMSTZ	−	
	RP02	INTPZ18	P0ACTLEDZ	CCS_BS1	−	
	RP03	INTPZ19	−	CCS_BS2	−	
	RP04	INTPZ20	P1ACTLEDZ	CCS_BS4	−	
	RP05	INTPZ21	−	CCS_BS8	−	
	RP06	WRZ2/BENZ2	HWRZ2/HBENZ2	-	−	
	RP07	WRZ3/BENZ3	HWRZ3/HBENZ3	−	−	
RP1	RP10	D24/HD24	−	−	−	Hi-Z With internal pull-up resistor
	RP11	D25/HD25	−	−	−	
	RP12	D26/HD26	−	−	−	
	RP13	D27/HD27	−	−	−	
	RP14	D28/HD28	−	−	−	
	RP15	D29/HD29	−	−	−	
	RP16	D30/HD30	−	−	−	
	RP17	D31/HD31	−	−	−	
RP2	RP20	BCYSTZ/ ADVZ	HBCYSTZ	−	−	Hi-Z With internal pull-up resistor
	RP21	A21	−	−	−	Hi-Z With internal pull-down resistor
	RP22	A22	−	−	−	
	RP23	A23	−	−	−	
	RP24	A24	INTPZ25	−	−	
	RP25	A25	INTPZ26	−	−	
	RP26	A26	INTPZ27	−	−	
	RP27	A27	INTPZ28	−	−	
RP3	RP30	D16/HD16	−	−	−	Hi-Z With internal pull-up resistor
	RP31	D17/HD17	−	−	−	
	RP32	D18/HD18	−	−	−	
	RP33	D19/HD19	−	−	−	
	RP34	D20/HD20	−	−	−	
	RP35	D21/HD21	−	−	−	
	RP36	D22/HD22	−	−	−	
	RP37	D23/HD23	−	−	−	

2.1.6 Serial Flash ROM Interface Signals

The Serial Flash ROM Interface supports Fast Read, Fast Read Dual Output and Fast Read Dual I/O mode.

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
SMSCK	O	Serial clock output port for serial flash ROM	P14	↑ / ↓	Hi-Z With internal pull-up resistor
SMSI	I/O	Serial data port for serial flash ROM (Connect to SO of serial flash ROM)	P15	High	
SMSO	I/O	Serial data port for serial flash ROM (Connect to SI of serial flash ROM)	P16	High	
SMCSZ	O	Chip select output port for serial flash ROM	P17	Low	

2.1.7 DMA Interface Signals

There are two DMA Controllers: one with four internal channels but only two external interfaces, and one with one internal channel and one external interce as real-time DMA controller.

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
RTDMAREQZ	I	RTDMAC DMA transfer request port	P62	Low	Hi-Z
RTDMAACKZ	O	RTDMAC DMA acknowledge output port	P63	Low	
RTDMATCZ	O	RTDMAC terminal count output port	P64	Low	
DMAREQZ0	I	DMA transfer request port 0	P65	Low	
DMAACKZ0	O	DMA acknowledge output port 0	P66	Low	
DMATCZ0	O	DMA Terminal count output port 0	P67	Low	
DMAREQZ1	I	DMA transfer request port 1	P32	Low	Hi-Z With internal pull-up resistor
DMAACKZ1	O	DMA acknowledge output port 1	P33	Low	
DMATCZ1	O	DMA Terminal count output port 1	P34	Low	

Caution Each DMA interface is assigned to a specific DMA channel.
DMA channel 0 = interface 0 (DMAREQZ0, DMAACKZ0, DMATCZ0)
DMA channel 1 = interface 1 (DMAREQZ1, DMAACKZ1, DMATCZ1)
DMA channels 2, 3 = no external interface

2.1.8 External Interrupt Input Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
NMIZ	I	Non-maskable external interrupt input port	-	Low	Hi-Z With internal pull-up resistor
INTPZ0-INTPZ5	I	External interrupt input port	P00-P05	Low	Hi-Z
INTPZ6, INTPZ7			P12,P13	Low	Hi-Z With internal pull-up resistor
INTPZ8-INTPZ10			P22-P24	Low	Hi-Z
INTPZ11			P43	Low	Hi-Z With internal pull-up resistor
INTPZ12-INTPZ15			P74-P77	Low	Hi-Z
INTPZ16-INTPZ21			RP00-RP05	Low	Hi-Z
INTPZ22-INTPZ24			P35-P37		With internal pull-up resistor
INTPZ25-INTPZ28			RP24-RP27		Hi-Z With internal pull-down resistor

2.1.9 Timer I/O Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
TIN0 / TOUT0	I/O	Timer TAUJ0 port	P27	-	Hi-Z
TIN1 / TOUT1	I/O	Timer TAUJ1 port	P26	-	
TIN2 / TOUT2	I/O	Timer TAUJ2 port	P57	-	Hi-Z With internal pull-up resistor
TIN3 / TOUT3	I/O	Timer TAUJ3 port	P52	-	Hi-Z With internal pull-down resistor

2.1.10 Watchdog Timer Output Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
WDTOUTZ	O	Watchdog Timer output port	P25	Low	Hi-Z

2.1.11 Trace Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
TRACECLK	O	Trace port clock output port	-	-
TRACEDATA3-TRACEDATA0	O	Trace port data output port	-	Low

2.1.12 CPU Power Control Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
SLEEPING	O	CPU SLEEP mode output port	P42	High	Hi-Z With internal pull-up resistor

2.1.13 Serial Interface Signals

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
TXD0	O	UART0 serial data output port	P21	-	Hi-Z
RXD0	I	UART0 serial data input port	P20	-	
TXD1	O	UART1 serial data output port	P31	-	Hi-Z
RXD1	I	UART1 serial data input port	P30	-	With internal pull-up resistor
CSISCK0	I/O	CSI0 serial clock port	P45	-	
CSISI0	I	CSI0 serial data input port	P46	-	
CSISO0	O	CSI0 serial data output port	P47	-	
CSICS00,CSICS01	O	CSI0 chip select 0,1 port	P70, P71	Low	Hi-Z
CSISCK1	I/O	CSI1 serial clock port	P35	-	Hi-Z
CSISI1	I	CSI1 serial data input port	P36	-	With internal pull-up resistor
CSISO1	O	CSI1 serial data output port	P37	-	
CSICS10,CSICS11	O	CSI1 chip select 0,1 port	P72, P73	Low	Hi-Z
SCL0	I/O	I2C0 serial clock port	P60	-	
SDA0	I/O	I2C0 serial data port	P61	-	
SCL1	I/O	I2C1 serial clock port	RP00	-	Hi-Z
SDA1	I/O	I2C1 serial data port	RP01	-	With internal pull-up resistor
CRXD0	I	CAN0 receive data port (5V-Tolerant buffer)	P53	-	
CTXD0	O	CAN0 transfer data port	P54	-	
CRXD1	I	CAN1 receive data port (5V-Tolerant buffer)	P55	-	
CTXD1	O	CAN1 transfer data port	P56	-	

2.1.14 CC-Link Signals (Intelligent device station)

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CCM_LINKERRZ	O	Link error LED control port	P20	Low	Hi-Z
CCM_ERRZ	O	Error LED control port	P21	Low	
CCM_RUNZ	O	RUN LED control port	P26	Low	
CCM_MDIN0-CCM_MDIN3	I	Mode setting switch input port	P62-P65	-	
CCM_SNIN0-CCM_SNIN7	I	Station No. setting switch port	P70-P77	-	
CCM_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCM_RDLEDZ	O	Receive data LED control port	P51	Low	
CCM_SDLEDZ	O	Transfer data LED control port	RP00	Low	
CCM_IRZ	O	Interrupt output port	P35	Low	
CCM_WDTENZ	I	Watchdog Timer error input port	P13	Low	
CCM_MSTZ	O	Operation check LED port	P37	Low	
CCM_SMSTZ	O	Stand-by master LED control port	RP01	Low	
CCM_RD	I	Data receive port	P53	-	
CCM_SD	O	Data transfer port	P54	-	
CCM_SDGCZ	O	Transfer data & gate control port	P42	Low	
CCM_CLK80M	I	CC-Link Clock	-	-	-

2.1.15 CC-Link Signals (Remote device station)

Caution To use a remote device station, it is necessary to connect a CCS_REFSTB terminal to an external interrupt terminal (INTPZ).

Pin Name	I/O	Function	Shared Port	Active	Level during reset & Level after reset
CCS_MON1- CCS_MON3	O	Monitor port	P32-P34	-	Hi-Z With internal pull-up resistor
CCS_MON4	O	Monitor port	P11	-	Hi-Z With internal pull-down resistor
CCS_MON0	O	Monitor port	P06	-	Hi-Z
CCS_MON5- CCS_MON7	O	Monitor port	P03-P05	-	
CCS_RESOUT	O	reset port	P07	High	
CCS_IOTENSU	I	Initial setting port	P22	-	
CCS_SENYU0	I	Initial setting port	P23	-	
CCS_SENYU1	I	Initial setting port	P24	-	
CCS_ERRZ	O	Operation check LED port	P25	Low	
CCS_RUNZ	O	Operation check LED port	P26	Low	
CCS_STATION_NO_0- CCS_STATION_NO_7	I	Station No. setting switch port	P70-P77	-	
CCS_LNKRUNZ	O	Link RUN LED control port	P50	Low	Hi-Z With internal pull-up resistor
CCS_REFSTB	O	Interrupt port	P10	High	
CCS_WDTZ	I	Watchdog Timer port	P13	Low	
CCS_RDLEDZ	O	Receive data LED control port	P51	Low	
CCS_RD	I	Data receive port	P53	-	
CCS_SD	O	Data transfer port	P54	-	
CCS_SDLEDZ	O	Operation check LED port	RP00	Low	
CCS_SDGATEON	O	Transfer data & gate control port	P52	High	Hi-Z With internal pull-down resistor
CCS_BS1	I	Baud rate setting switch port	RP02	-	Hi-Z With internal pull-up resistor
CCS_BS2	I	Baud rate setting switch port	RP03	-	
CCS_BS4	I	Baud rate setting switch port	RP04	-	
CCS_BS8	I	Baud rate setting switch port	RP05	-	
CCS_FUSEZ	I	Fuse cutting signal port	P36	Low	
CCM_CLK80M	I	CC-Link clock	-	-	-

2.1.16 System Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
XT1	I	Crystal Oscillator for system clock connect port	-	-
XT2	I/O	*Oscillator output connects to X2 in the case of connecting it directly.	-	-
RESETZ	I	Reset input port	Low	-
PONRZ	I	Internal RAM Power on reset input port	Low	-
OSCTH	I	Input High level when external clock input mode	-	-
JTAGSEL	I	JTAG Operation mode setting port	-	-
RSTOUTZ	O	Reset to external circuit output port	Low	-
PLL_VDD	-	PLL power supply (1.0V)	-	-
PLL_GND	-	PLL power Ground supply (GND)	-	-
VDD33	-	I/O power supply (3.3V)	-	-
VDD10	-	Internal power supply (1.0V)	-	-
GND	-	Ground supply (GND)	-	-
LX	O	Regulator 1.5V power Output	-	-
EXTRES	-	Reference resistor for EtherPHY connect port	-	-
P0VDDARXTX	-	Analog Port Rx/Tx power supply(1.5V) - Port 0	-	-
P1VDDARXTX	-	Analog Port Rx/Tx power supply(1.5V) - Port 0	-	-
VDDACB	-	EtherPHY Analog Central power supply (3.3V)	-	-
AGND	-	EtherPHY Analog Ground supply (GND)	-	-
VDD15	-	EtherPHY I/O for EtherPHY power supply (1.5V)	-	-
VDDAPLL	-	EtherPHY Analog Central power supply (1.5V)	-	-
VSSAPLLCB	-	EtherPHY Analog Central Ground supply (GND)	-	-
VDD33ESD	-	EtherPHY Analog Test power supply (3.3V)	-	-
AVDD_REG	-	Regulator Analog power supply(3.3V)	-	-
AGND_REG	-	Regulator Analog Ground supply (GND)	-	-
BVDD	-	Regulator power supply (3.3V)	-	-
BGND	-	Regulator Ground supply (GND)	-	-
FB	I	Regulator Feedback port	-	-
VDDQ_PECL_B0	-	PECL Buffer power supply (3.3V)	-	-
VDDQ_PECL_B1	-	PECL Buffer power supply (3.3V)	-	-

2.1.17 Test Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
TMODE0-TMODE2	I	Test mode select port	-	-
TMS	I/O	JTAG mode select port	-	-
TDI	I	JTAG serial data input port	-	-
TDO	O	JTAG serial data output port	-	-
TRSTZ	I	JTAG reset port	Low	-
TCK	I	JTAG clock input port	-	-
ATP[Note]	I	Renesas test port		
TMC1	I		-	-
TMC2	I		-	-
TEST1[Note]	I		-	-
TEST2[Note]	I		-	-
TEST3[Note]	I		-	-
TESTOUT5[Note]	O		-	-

2.1.18 Operation mode Setting Signals

Pin Name	I/O	Function	Active	Level during reset & Level after reset
BOOT1-BOOT0	I	Boot mode select port 00 : External memory boot 01 : External serial flash ROM boot 10 : External MPU boot 11 : Instruction RAM boot(debugger used ONLY)	-	-
MEMIFSEL	I	External Memory Interface select port 0 : Slave memory Interface 1 : External MPU Interface	-	-
BUS32EN	I	External Memory Interface Bus width select port 0 : 16bit bus 1 : 32bit bus	-	-
HIFSYNC	I	External MPU I/F Operation mode select port 0 : asynchronous SRAM Interface 1 : synchronous SRAM Interface	-	-
HWRZSEL	I	External MPU Interface HWRZ/HBENZ select port 0 : HBENZ use 1 : HWRZ use	-	-
MEMCSEL	I	Internal Memory Controller select port 0 : asynchronous SRAM MEMC 1 : synchronous burst access MEMC	-	-
ADMUXMODE	I	Multiplex of Address / Data port [Note] 0 : Separate 1 : Multiplex of Address / Data	-	-

Note. ADMUXMODE port is only available when MEMCSEL port is High (which selects synchronous burst access MEMC). The asynchronous SRAM MEMC does not support address/data multiplexing.

2.2 Port status

The initial status of Port function after the reset cancellation varies according to the status of the operation mode setting signal.

Port Name	External memory boot				External MPU boot		External Serial Flash ROM boot
	Asynchronous MEMC		Synchronous burst MEMC				
	16bit	32bit	16bit	32bit	16bit	32bit	
P14	P14	P14	P14	P14	P14	P14	SMSCK
P15	P15	P15	P15	P15	P15	P15	SMSI
P16	P16	P16	P16	P16	P16	P16	SMSO
P17	P17	P17	P17	P17	P17	P17	SMCSZ
P40	A1	P40	A1	A1	HA1	P40	P40
P41	P41	P41	P41	P41	HWAITZ	HWAITZ	P41
P42	P42	P42	P42	P42	HERROUTZ	HERROUTZ	P42
P43	P43	P43	P43	P43	HBUSCLK	HBUSCLK	P43
P44	P44	P44	P44	P44	HPGCSZ	HPGCSZ	P44
RP06	RP06	WRZ2/ BENZ[note1]	RP06	WRZ2/ BENZ[note1]	RP06	HWRZ2/ HBENZ[note2]	RP06
RP07	RP07	WRZ3/ BENZ[note1]	RP07	WRZ3/ BENZ[note1]	RP07	HWRZ3/ HBENZ[note2]	RP07
RP20	RP20	RP20	ADVZ	ADVZ	HBCYSTZ	HBCYSTZ	RP20
RP10-RP17	RP10-RP17	D24-D31	RP10-RP17	D24-D31	RP10-RP17	HD24-HD31	RP10-RP17
RP30-RP37	RP30-RP37	D16-D23	RP30-RP37	D16-D23	RP30-RP37	HD16-HD23	RP30-RP37

Note1. When using asynchronous SRAM MEMC, WRZ[3:0] and BENZ[3:0] are converted by WREN register. In addition, when using synchronous burst MEMC, WRZ[3:0] and BENZ[3:0] are converted by OPMODE register.

Note2. HWRZ[3:0] and HBENZ[3:0] are converted by the level of HWRZSEL port.

2.3 Buffer Type and Recommended Connection of Unused Pins

2.3.1 Ethernet Signals

(1) Media Interface Signal

Pin Name	I/O	Interface	Recommended connection when not in use
P0_RX_P	I	3.3V Analog Input Buffer	Open
P0_RX_N	I		
P1_RX_P	I		
P1_RX_N	I		
P0_TX_P	O	3.3V Analog Output Buffer	Open
P0_TX_N	O		
P1_TX_P	O		
P1_TXN	O		
P0_SD_P	I	3.3V PECL Input Buffer	Connect to GND
P0_SD_N	I		
P1_SD_P	I		
P1_SD_N	I		
P0_RD_P	I		
P0_RD_N	I		
P1_RD_P	I		
P1_RD_N	I		
P0_TD_OUT_P	O	3.3V PECL Output Buffer	Open
P0_TD_OUT_N	O		
P1_TD_OUT_P	O		
P1_TD_OUT_N	O		
P0_FX_EN_OUT	O	Output Buffer (3.3V) 12mA	Open
P1_FX_EN_OUT	O		

2.3.2 External Memory/ MPU Interface Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BUSCLK	O	Output Buffer (3.3V) 9mA	Open
CSZ0 / HCSZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
A2-A20 / HA2-HA20	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-down	Open
D0-D15 / HD0-HD15			
RDZ / HRDZ	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
WRSTBZ / HWRSTBZ			
WRZ0, WRZ1 / BENZ0, BENZ1 / HWRZ0, HWRZ1			

2.3.3 System Signals

Pin Name	I/O	Interface	Recommended connection when not in use
NMIZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Connect to VDD33(3.3V)
XT1	I	Oscillator with EN	Connect to GND
XT2	-		-
RSTOUTZ	O	Output Buffer (3.3V) 6mA	Open
RESETZ	I	Input Buffer (3.3V) Schmitt in	-
PONRZ			
OSCTH		Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	Connect to VDD33(3.3V)
JTAGSEL			

2.3.4 Test Signals

Pin Name	I/O	Interface	Required Connection when not in use
TMODE0-TMODE2	I	Input Buffer (3.3V) Schmitt in, 50kΩ Pull-down	Connect to GND
TMS	I/O	I/O Buffer (3.3V) 6mA 50kΩ Pull-up	Open
TDI	I	Input Buffer (3.3V) , 50kΩ Pull-up	Open
TDO	O	3-state Output Buffer (3.3V) 6mA	Open
TRSTZ	I	Input Buffer (3.3V) Schmitt in 50kΩ Pull-up	Open
TCK	I	Input Buffer (3.3V) , 50kΩ Pull-down	Open
TMC1	I	(TMC1) Input Buffer (3.3V) for TMC Terminal	Connect to GND
TMC2	I	(TMC2) Input Buffer (3.3V) for TMC Terminal	Connect to GND
ATP	I	Input Buffer (3.3V)	Open
TEST1	I	Input Buffer (3.3V)	Connect to GND
TEST2	I	Input Buffer (3.3V)	
TEST3	I	Input Buffer (3.3V)	
TESTDOUT5	O	Output Buffer（3.3V）	Open

2.3.5 Port Signals

(1/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P00-P07	I/O	I/O Buffer (3.3V) (6mA)	Connect to GND
P10	I/O	Programmable I/O Buffer (3.3V) (6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
P11-P17	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P20-P27	I/O	I/O Buffer (3.3V) (6mA)	Connect to GND
P30-P36	I/O	Programmable I/O Buffer (3.3V) (6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
P37	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P40-P47	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P50-P51	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P52	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	
P53-P56	I/O	5V-tolerant I/O Buffer 4mA 50kΩ Pull-up	Open
P57	I/O	Programmable I/O Buffer (3.3V)(6mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
P60-P67	I/O	I/O Buffer (3.3V) (6mA)	Connect to GND

(2/2)

Pin Name	I/O	Interface	Recommended connection when not in use
P70-P77	I/O	I/O Buffer (3.3V) (6mA)	Connect to GND
RP00-RP07	I/O	Programmable I/O Buffer (3.3V) Load Drive select function (6mA, 12mA) Resistor select function (50kΩ Pull-up or 50kΩ Pull-down or less)	Open
RP10-RP17			
RP20-RP27			
RP30-RP37			

2.3.6 Operation Mode Setting Signals

Pin Name	I/O	Interface	Recommended connection when not in use
BOOT0, BOOT1	I	Input Buffer (3.3V) Schmitt in	-
MEMIFSEL			
BUS32EN			
HIFSYNC			
HWRZSEL			
MEMCSEL			
ADMUXMODE			

2.3.7 CC-Link Master Signal (Intelligent device station, Remote device station)

Pin Name	I/O	Interface	Recommended connection when not in use
CCM_CLK80M	I	Input Buffer (3.3V)	Connect to GND

2.3.8 Trace Signals

Pin Name	I/O	Interface	Recommended connection when not in use
TRACECLK	O	Output Buffer (3.3V) 6mA	Open
TRACEDATA[3:0]			

3. Memory Maps

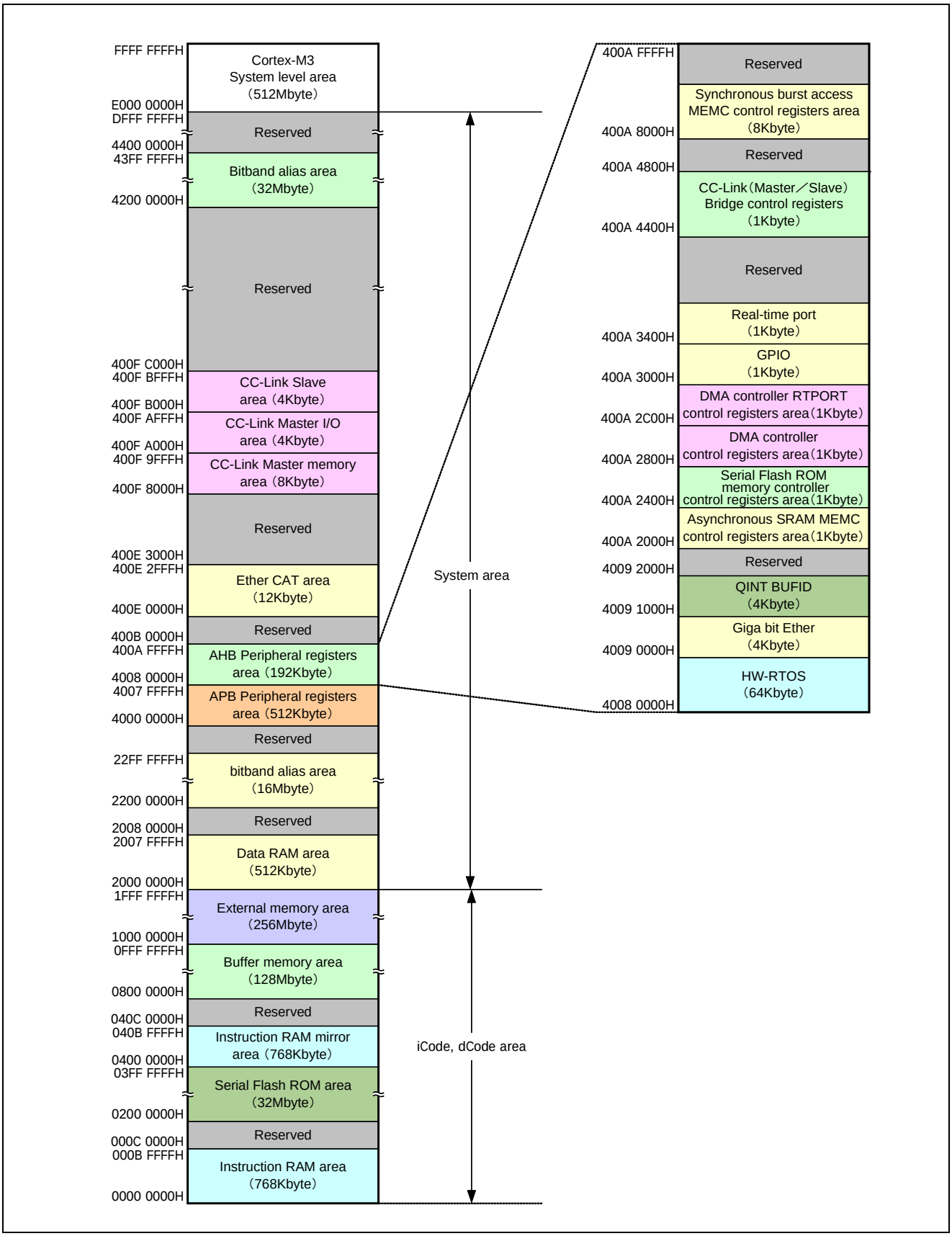

Figure 3.1 Memory map (ALL)

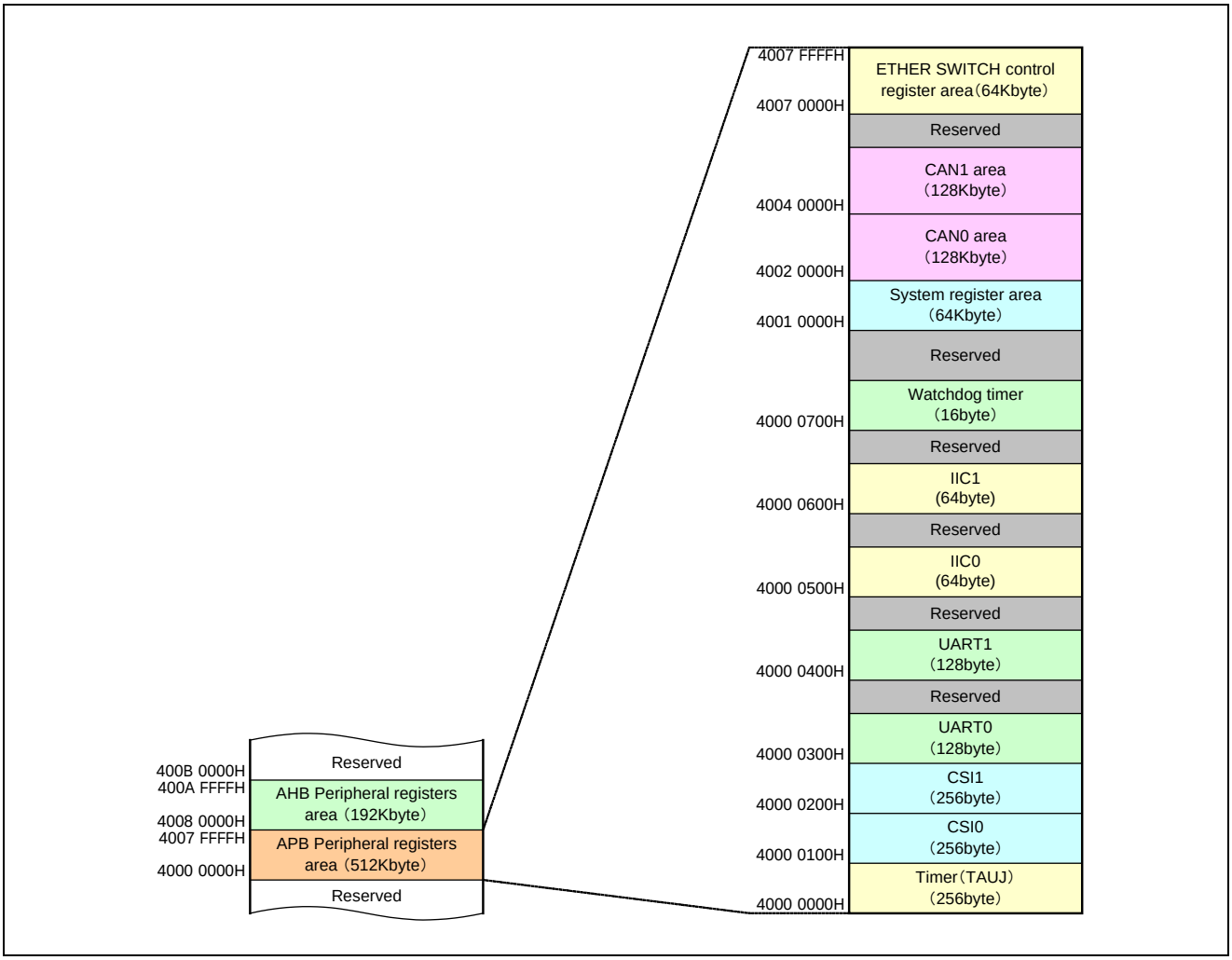

Figure 3.2 Memory map (APB Peripheral registers area)

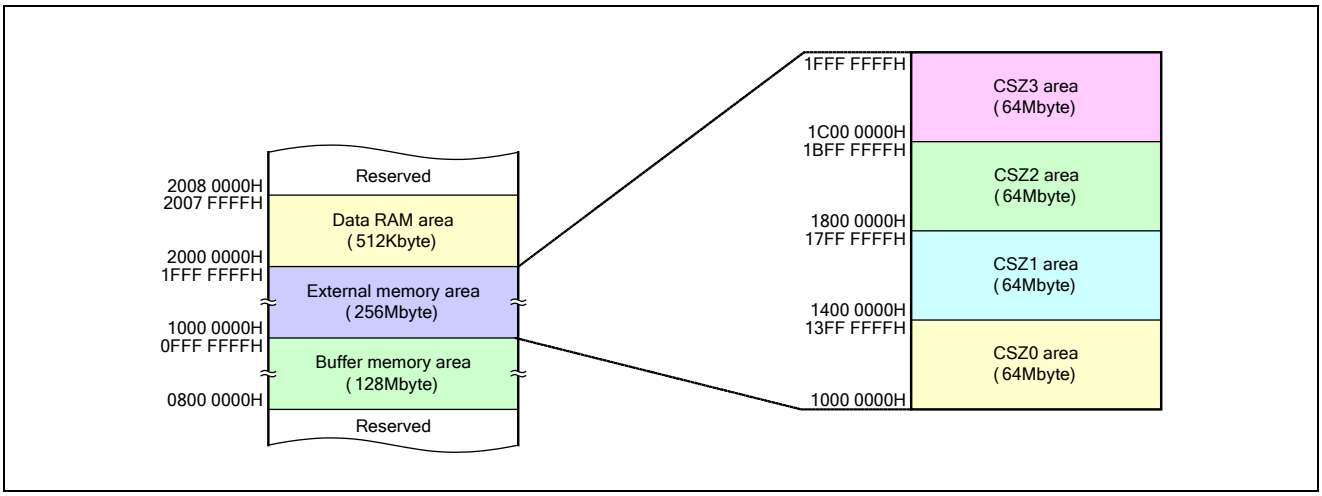

Figure 3.3 Memory map (External memory area)

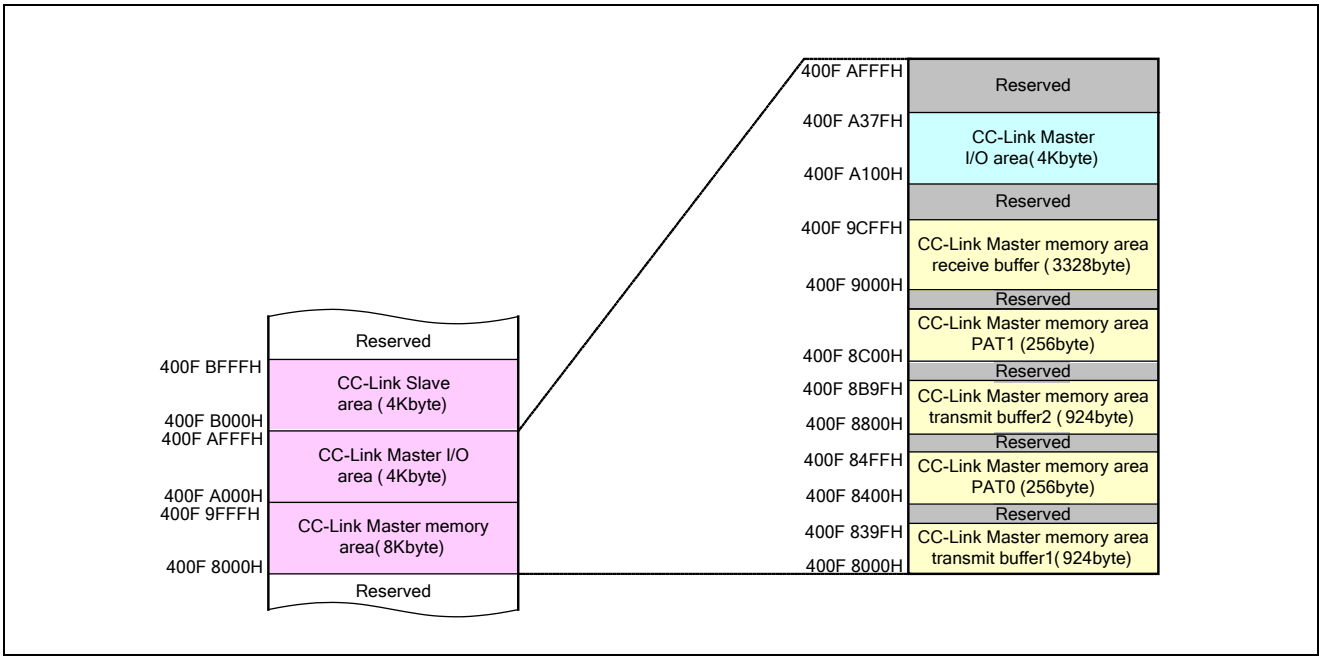

Figure 3.4 Memory map (CC-Link Master area)

Caution1. CC-Link Master shows function block of Intelligent station.

Caution2. CC-Link Slave shows function block of remote device station.

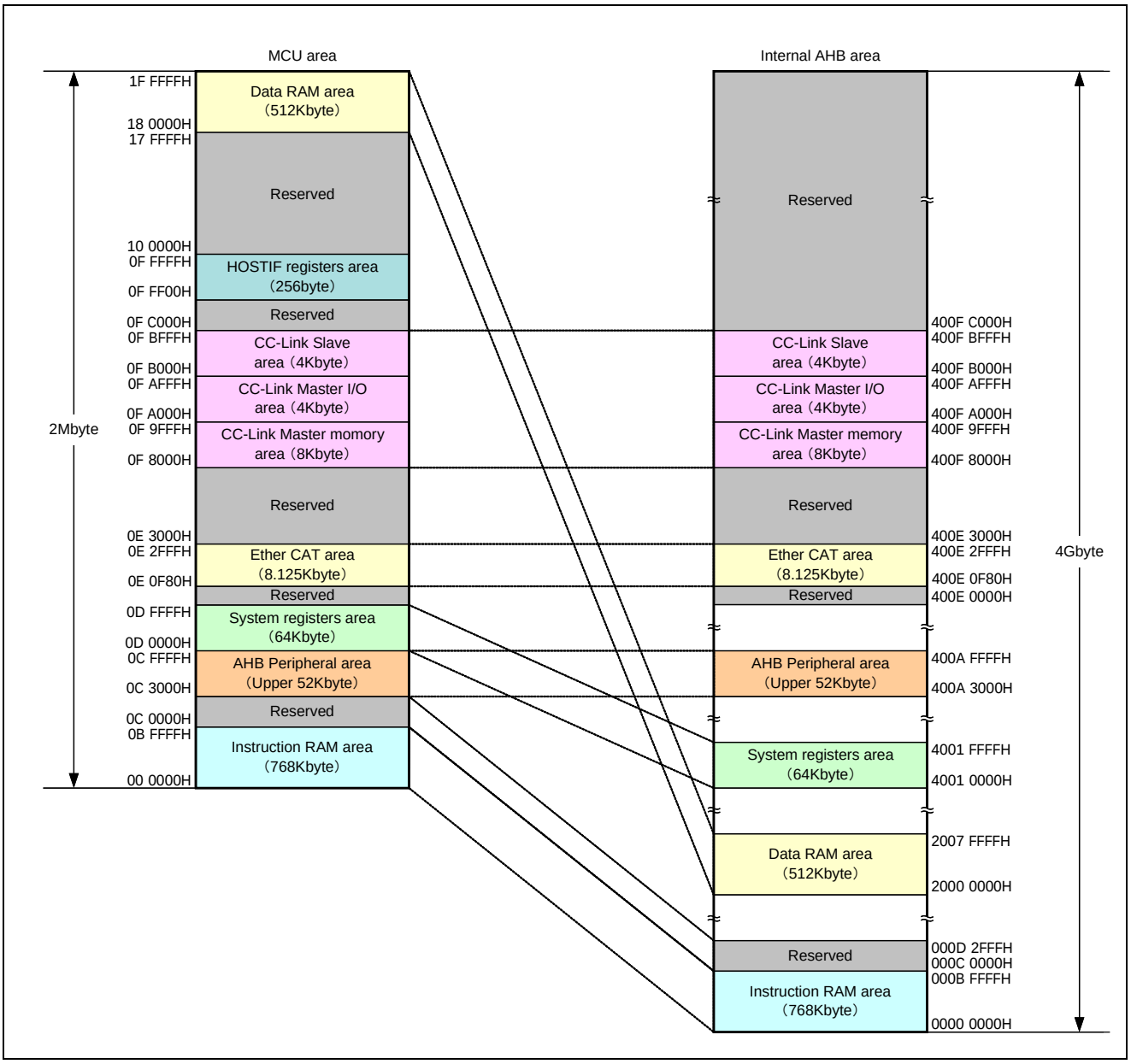

Figure 3.5 External MPU interface area

4. Exception handling function

R-IN32M3 use the Interrupt Controller built-in to Cortex-M3

Please refer to the following URL of ARM for Exceptions handling operation of Cortex-M3.

http://infocenter.arm.com/help/topic/com.arm.doc.set.cortexm/index.html

4.1 Exceptions list

Exception No.1-15 is system exception of Cortex-M3 CPU. The interrupt from the internal hardware of R-IN32M3 and External port is assigned after Exception No.16.

Exception No.	Exception type	Priority	Remark
1	Reset	-3 (most significant)	-Reset port (RST_B) input -Reset from Watchdog Timer -Set (1) the SYSRESETREQ bit of NVIC built-in Cortex-M3 CPU
2	NMI	-2	-NMI port input -Generate NMI from Watchdog Timer
3	Hard fault	-1	Using to the promotion of exception fault of all class that can be operated by other exceptions.
4	Memory manage fault	programmable	Exception from MPU
5	Bus fault	programmable	Bus error of bus access to the area that is not controlled by MPU
6	Use fault	programmable	Error about operating instruction including undefined instruction
7~10	Reserved	-	-
11	SVCall	programmable	Call of system service by SVC interrupt
12	Debug Monitor	programmable	Debug Monitor
13	Reserved	-	-
14	PendSV	programmable	Request to system service that can be reserved
15	SysTick	programmable	Indication from system timer
16~	R-IN32M3 specific Interrupt	programmable	Interrupt from the internal hardware of R-IN32M3 and External port.

4.2 Interrupt list

This interrupt is exception(interrupt) after the Exception No.16 that is assigned NVIC of Cortex-M3 CPU.

In R-IN32M3, the interrupts from the internal hardware of R-IN32M3 and external port connect to not only NVIC of Cortex-M3 but also the internal Hardware Real-time OS,.starting trigger of internal DMAC and timer.

R-IN32M3 support the following interrupts.

Table4.1 Interrupt list

(1/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
16	INTTAUJ2I0	Timer array TAUJ2 channel 0 interrupt	○	○	○	○	○
17	INTTAUJ2I1	Timer array TAUJ2 channel 1 interrupt	○	○	○	○	○
18	INTTAUJ2I2	Timer array TAUJ2 channel 2 interrupt	○	○	○	○	○
19	INTTAUJ2I3	Timer array TAUJ2 channel 3 interrupt	○	○	○	○	○
20	INTUAJ0TIT	UARTJ0 transmission interrupt	○	○	○	○	○
21	INTUAJ0TIR	UARTJ0 reception interrupt	○	○	○	○	○
22	INTUAJ1TIT	UARTJ1 transmission interrupt	○	○	○	○	○
23	INTUAJ1TIR	UARTJ1 reception interrupt	○	○	○	○	○
24	INTCSIH0IC	CSIH0 communication status interrupt	○	○	○	○	○
25	INTCSIH0IR	CSIH0 reception status interrupt	○	○	○	○	○
26	INTCSIH0IJC	CSIH0 end of job interrupt	○	○	○	○	○
27	INTCSIH1IC	CSIH1 communication status interrupt	○	○	○	○	○
28	INTCSIH1IR	CSIH1 reception status interrupt	○	○	○	○	○
29	INTCSIH1IJC	CSIH1 end of job interrupt	○	○	○	○	○
30	INTIICB0TIA	IICB0 transmission/reception interrupt request	○	○	○	○	○
31	INTIICB1TIA	IICB1 transmission/reception interrupt request	○	○	○	○	○
32	INTFCN0REC	FCN0 reception completion	○	○	○	○	○
33	INTFCN0TRX	FCN0 transmission completion	○	○	○	○	○
34	INTFCN0WUP	FCN0 sleep and wakeup / transmission suspension	○	○	○	○	○
35	INTFCN1REC	FCN1 reception completion	○	○	○	○	○
36	INTFCN1TRX	FCN1 transmission completion	○	○	○	○	○
37	INTFCN1WUP	FCN1 sleep and wakeup / transmission suspension	○	○	○	○	○
38	INTDMA00	DMAC channel0 transfer completion interrupt	○	○	○	○	○
39	INTDMA01	DMAC channel1 transfer completion interrupt	○	○	○	○	○
40	INTDMA02	DMAC channel2 transfer completion interrupt	○	○	○	○	○
41	INTDMA03	DMAC channel3 transfer completion interrupt	○	○	○	○	○
42	INTRTDMA	RTDMAC transfer completion interrupt	○	○	○	○	○
43	INTCATSYNC0	EtherCAT Sync0 interrupt	○	○	○	○	-
44	INTCATSYNC1	EtherCAT Sync1 interrupt	○	○	○	○	-
45	INTCAT	EtherCAT interrupt	○	○	○	○	○

(2/4)

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
46	INTCATSOF	EtherCAT SOF interrupt	○	○	○	○	○
47	INTCATEOF	EtherCAT EOF interrupt	○	○	○	○	○
48	INTBUFDMA	Inter-Buffer DMA transfer completion	○	○	○	○	○
49	INTPHY0	Ether PHY interrupt0	○	○	○	○	○
50	INTPHY1	Ether PHY interrupt1	○	○	○	○	○
51	INTETHMII	Ether MII management access completion interrupt	○	○	○	○	○
52	INTETHPAUSE	Ether pause packet transmission completion	○	○	○	○	○
53	INTETHTX	Ether transmission completion interrupt	○	○	○	○	○
54	INTETHSW	Ether SWITCH interrupt	○	○	○	○	○
55	INTETHSWDLR	Ether SWITCH DLR interrupt	○	○	○	○	○
56	INTETHSWSEC	Ether SWITCH SEC interrupt	○	○	○	○	○
57	INTETHRXFIFO	RX FIFO overflow	○	○	-	-	-
58	INTETHTXFIFO	TX FIFO underflow	○	○	-	-	-
59	INTETHRXDMA	Ether MACDMA reception completion	○	○	○	○	○
60	INTETHTXDMA	Ether MACDMA transmission completion	○	○	○	○	○
61	INTMACDMARXFRM	receive frame successfully interrupt	○	○	○	○	○
62	INTHOSTIF	External MPU I/F interrupt	○	○	○	○	○
63	INTPZ0	INTPZ0 input	○	○	○	○	○
64	INTPZ1	INTPZ1 input	○	○	○	○	○
65	INTPZ2	INTPZ2 input	○	○	○	○	○
66	INTPZ3	INTPZ3 input	○	○	○	○	○
67	INTPZ4	INTPZ4 input	○	○	○	○	○
68	INTPZ5	INTPZ5 input	○	○	○	○	○
69	INTPZ6	INTPZ6 input	○	○	○	○	○
70	INTPZ7	INTPZ7 input	○	○	○	○	○
71	INTPZ8	INTPZ8 input	○	○	○	○	○
72	INTPZ9	INTPZ9 input	○	○	○	○	○
73	INTPZ10	INTPZ10 input	○	○	○	○	○
74	INTPZ11	INTPZ11 input	○	○	○	○	○
75	INTPZ12	INTPZ12 input	○	○	○	○	○
76	INTPZ13	INTPZ13 input	○	○	○	○	○
77	INTPZ14	INTPZ14 input	○	○	○	○	○
78	INTPZ15	INTPZ15 input	○	○	○	○	○
79	INTPZ16	INTPZ16 input	○	○	○	○	○
80	INTPZ17	INTPZ17 input	○	○	○	○	○
81	INTPZ18	INTPZ18 input	○	○	○	○	○
82	INTPZ19	INTPZ19 input	○	○	○	○	○

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Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
83	INTPZ20	INTPZ20 input	○	○	○	○	○
84	INTPZ21	INTPZ21 input	○	○	○	○	○
85	INTPZ22	INTPZ22 input	○	○	○	○	○
86	INTPZ23	INTPZ23 input	○	○	○	○	○
87	INTPZ24	INTPZ24 input	○	○	○	○	○
88	INTPZ25	INTPZ25 input	○	○	○	○	○
89	INTPZ26	INTPZ26 input	○	○	○	○	○
90	INTPZ27	INTPZ27 input	○	○	○	○	○
91	INTPZ28	INTPZ28 input	○	○	○	○	○
92	INTHWRTOS	HW-RTOS interrupt	○	-	-	-	-
93	INTBRAMERR	Buffer RAM area access error	○	○	-	-	-
94	INTIICB0TIS	I2C0 status interrupt	○	○	-	-	-
95	INTIICB1TIS	I2C1 status interrupt	○	○	-	-	-
96	-	Reserve	-	-	-	-	-
97	INTSFLASH	Serial Flash ROM controller error interrupt	○	○	-	-	-
98	INTUAJ0TIS	UARTJ0 status interrupt	○	○	-	-	-
99	INTUAJ1TIS	UARTJ1 status interrupt	○	○	-	-	-
100	INTCSIH0IRE	CSIH0 communication error interrupt	○	○	-	-	-
101	INTCSIH1IRE	CSIH1 communication error interrupt	○	○	-	-	-
102	INTFCN0ERR	FCN0 error detection	○	○	-	-	-
103	INTFCN1ERR	FCN1 error detection	○	○	-	-	-
104	INTDERR0	DMAC error response interrupt	○	○	-	-	-
105	INTDERR1	RTDMAC error response interrupt	○	○	-	-	-
106	INTETHTXFIFOERR	TX-FIFO error interrupt	○	○	-	-	-
107	INTETHRXERR	Ether receive flame error	○	○	-	-	-
108	INTETHRXDERR	MACDMA reception error interrupt	○	○	-	-	-
109	INTETHTXDERR	MACDMA transmission error interrupt	○	○	-	-	-
110	INTBUFDMAERR	Internal Buffer DMA error	○	○	-	-	-
111	-	Reserve	-	-	-	-	-
112	INTECATRST	EtherCAT RESET interrupt	○	○	-	-	-
113	-	Reserve	-	-	-	-	-
114	-	Reserve	-	-	-	-	-
115	-	Reserve	-	-	-	-	-
116	-	Reserve	-	-	-	-	-
117	-	Reserve	-	-	-	-	-
118	-	Reserve	-	-	-	-	-
119	-	Reserve	-	-	-	-	-

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Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
120	-	Reserve	-	-	-	-	-
121	-	Reserve	-	-	-	-	-
122	-	Reserve	-	-	-	-	-
123	-	Reserve	-	-	-	-	-
124	-	Reserve	-	-	-	-	-
125	-	Reserve	-	-	-	-	-
126	-	Reserve	-	-	-	-	-
127	-	Reserve	-	-	-	-	-
128	-	Reserve	-	-	-	-	-
129	-	Reserve	-	-	-	-	-
130	-	Reserve	-	-	-	-	-
131	INTCCMRQ	CC-Link INTRQ interrupt	○	○	○	○	○
132	INTCCSRFSTB	CC-Link RFSTB interrupt Note	○	○	○	○	○
133	INTCCSMON3	CC-Link MON3 interrupt	○	○	○	○	○

Note To use a CC-Link remote device station(V2.0), INTCCSRFSTB can not be used. It is necessary to connect a CCS_REFSTB(P10) terminal to an external interrupt terminal (INTPZ).

5. Peripheral function

Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of following peripheral functions.

- Clock function
- CPU
- Bus structure
- Hardware Real-time OS
- Giga bit Ethernet I/F
- Asynchronous SRAM MEMC
- Synchronous burst access MEMC
- Serial Flash ROM MEMC
- DMA function
- Timer Array Unit J (TAUJ)
- Window Watchdog Timer A (WDTA)
- Asynchronous Serial Interface J (UARTJ)
- Clocked Serial Interface H (CSIH)
- I2C BUS (IICB)
- CAN Controller (FCN)
- CC-Link (Intelligent device station)
- CC-Link (Remote device station)
- Other I/F control
- Debug function

6. EtherCAT Slave Controller function

6.1 Features

The EtherCAT Slave Controller (ESC) core is made by Beckhoff Automation GmbH, Germany.

The ESC processes EtherCAT communications and acts as interface between EtherCAT Field bus and Slave applications.

Table 6.1 Features of EtherCAT Slave Controller

Feature	R-IN32M3-EC	ET1100	Remark
Ports	2	2-4	-
FMMUs	8	8	-
SyncManagers	8	8	-
Process Data RAM [KByte]	8	8	-
Distributed Clocks	64bit	64bit	-
EBus	No	Yes (0-4)	-
Process Data Interfaces			
Digital I/O	No	Yes	-
SPI Slave	No	Yes	
Host MPU Interface	On-chip bus (SRAM Host Interface)	8bit/16bit, async./sync.	

Caution. Register area (0E_0000H-0E_0F7FH) can't be accessed from the external MPU I/F.

6.2 Peripheral circuit of EtherCAT

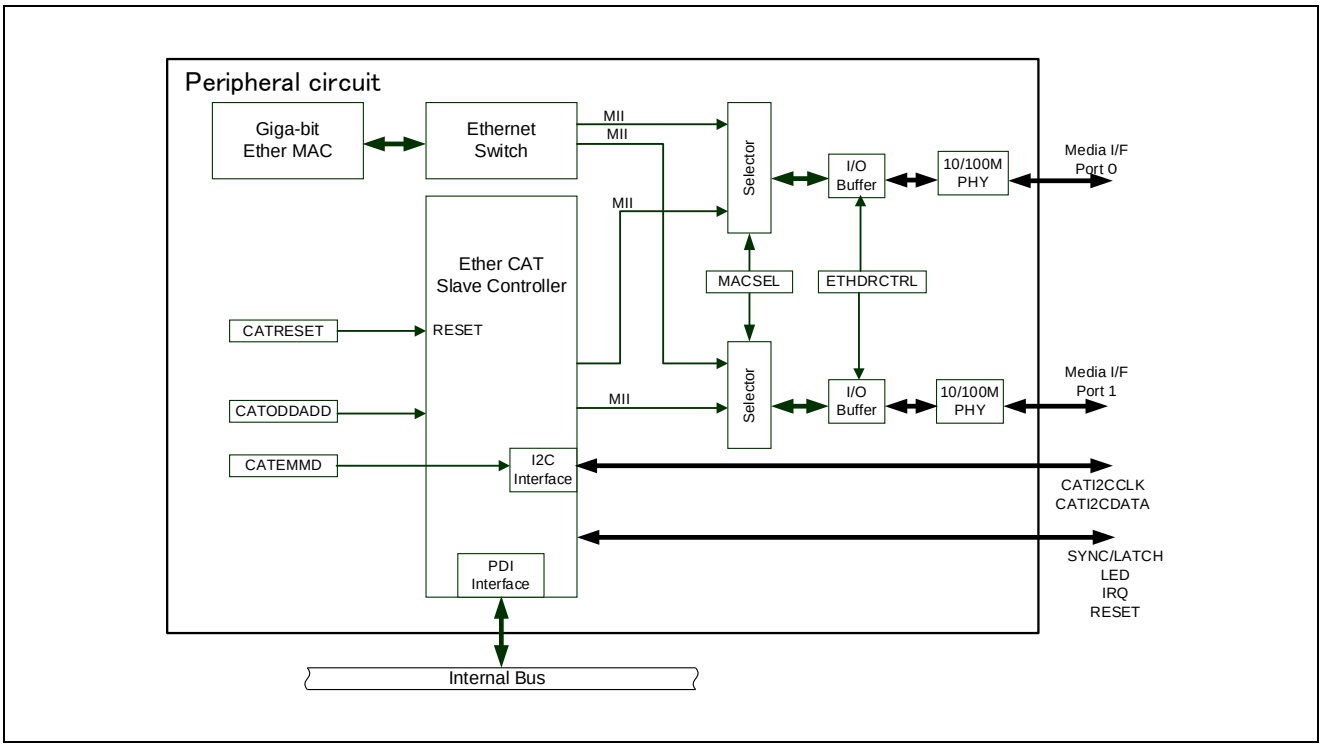

Figure 6.1 Peripheral circuit of EtherCAT

6.3 Interrupt list and I/O signals

Table 6.2 Interrupt list of EtherCAT Slave Controller

Exception No.	Name	Cause group	Connection				
			NVIC	HW-RTOS	DMAC	Real Time Port	Timer
43	INTCATSYNC0	EtherCAT Sync0 interrupt	○	○	○	○	-
44	INTCATSYNC1	EtherCAT Sync1 interrupt	○	○	○	○	-
45	INTCAT	EtherCAT interrupt	○	○	○	○	○
46	INTCATSOF	EtherCAT SOF interrupt	○	○	○	○	○
47	INTCATEOF	EtherCAT EOF interrupt	○	○	○	○	○
112	INTECATRST	EtherCAT RESET interrupt	○	○	-	-	-

Table 6.3 I/O signals of EtherCAT Slave Controller (excluding PHY MDI signals)

Pin Name	I/O	Function	Shared Port	Active
CATLEDRUN	O	Ether CAT RUN LED port	P00	High
CATIRQ	O	Ether CAT IRQ port	P01	High
CATLEDSTER	O	Ether CAT Dual-color State LED port	P02	High
CATLEDERR	O	Ether CAT Error LED port	P03	High
CATLINKACT0,	O	Ether CAT Link / Activity LED port (Port 0)	P04	High
CATLINKACT1	O	Ether CAT Link / Activity LED port (Port 1)	P05	High
CATSYNC0	O	Ether CAT SYNC0 port	P11	High
CATSYNC1	O	Ether CAT SYNC1 port	P10	High
CATLATCH0	I	Ether CAT LATCH0 port	P11	High
CATLATCH1	I	Ether CAT LATCH1 port	P10	High
CATI2CCLK	O	Ether CAT EEPROM I2C clock port	P22	-
CATI2CDATA	I/O	Ether CAT EEPROM I2C data port	P23	-
CATRESTOUT	O	Ether CAT PHY RESETOUT port	P56	-

6.4 Functional Overview

Typical functions of EtherCAT Slave Controller and supported function by R-IN32M3-EC are shown below. Regarding the detailed specification of EtherCAT and ESC, refer to the documentation (e.g. ETG.1000 EtherCAT Specification) provided by EtherCAT Technology Group (ETG) and the EtherCAT Slave Controller IP Core (v2.04) datasheet provided by Beckhoff Automation.

Table 6.4 Typical functions of EtherCAT Slave Controller and supported function by R-IN32M3-EC

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Features	Functions	Support
EtherCAT Protocol	Handling the following frames: ・Ethernet frames with Ether type 0x88A4 ・EtherCAT frames encapsulated in UDP/IP ・EtherCAT frames with VLAN Tag ・Normal Ethernet frames	○
Addressing Modes	Device Addressing ・Auto Increment Address ・Configured Station Address ・Broadcast	○
	Logical Addressing	○
Working Counter	Counting the number of Read/Write from/to the device	○
EtherCAT Command Types	Processing the command that master requests slaves to address each addressing mode	○
Loop Control	Loop Control and Loop State	○
Shadow buffers	Shadow buffers function when register is written	○
Circulating Frames	Processing of circulating frames during the failure	○
Link Detection	Link MII signal	○
	MI Link Detection and Configuration	○
	Enhanced Link Detection	○
FIFO size reduction	RX FIFO size reduction because of reduction of propagation delay	○
Ethernet Physical Layer	MII	-
	MDI (100BASE-TX)	○
	MDI (100BASE-FX)	-
	EBUS	-
	Back-to-Back MII connection	-
	MII Management Interface	○
	Read/Write of the PHY register via MII Management Interface	○
	PHY address offset	○
	Manual TX clock shift compensation	-
	Automatic TX clock shift compensation	○
FMMU	Mapping between logical address and physical address	○
SyncManager	Buffered Mode	○
	Mailbox Mode	○
	Interrupt and latch event generation when a buffer was completely and successfully written or read.	○
	Repeating Mailbox Communication	○
	SyncManager Deactivation by the PDI	○

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Features	Functions	Support
Distributed Clocks	Clock Synchronization considering propagation delay and drift compensation	○
	Generation of synchronous output signals (SyncSignals) ・Cyclic Generation ・Single Shot Mode ・Cyclic Acknowledge Mode ・Single Shot Acknowledge Mode	○
	Precise time stamping of input events (LatchSignals) ・Single Event Mode ・Continuous Mode ・SyncManager Event	○
	Generation of synchronous interrupts	○
	Synchronous Digital Output updates / Synchronous Digital Input sampling	-
	ECAT or PDI Control Sync signals / Latch signals.	○
	System Time PDI Controlled	-
	Communication Timing ・Free Run ・Synchronized to Output Event ・Synchronized to SyncSignal	○
EtherCAT State Machine	Control of State Machine / Indication of the Status and error code	○
	Device Emulation	-
SII EEPROM	SII EEPROM Commands	○
	SII EEPROM Error Indication	○
	SII EEPROM Access Interface	○
	EEPROM Size selection	○
	EEPROM Emulation	-
Interrupt	AL Event Request (PDI Interrupt)	○
	ECAT Event Request (ECAT Interrupt)	○
Watchdog	Process Data Watchdog	○
	PDI Watchdog	○
Error Counters	Port Error Counters	○
	Forwarded RX Error Counter	○
	ECAT Processing Unit Error Counter	○
	PDI Error Counter	○
	Lost Link Counter	○
	Watchdog Counter Process Data	○
	Watchdog Counter PDI	○
LED signals	RUN LED signal	○
	ERR LED signal	○
	STATE LED and STATE_RUN LED signal	○
	LINK/ACT LED signals	○
	Port Error LED (PERR)	-
	RUN/ERR LED Override	○

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Features	Functions	Support
Process Data Interface (PDI)	Digital I/O	-
	SPI slave	-
	8b/16b sync./async. µC	-
	On-chip bus	○
	General Purpose I/O	-
Write Protection	Active register write protection (0x0000-0x0FFF)	○
	Active ESC write protection (0x0000-0x2FFF)	○
ESC Reset	ESC reset from master or PDI	○

6.5 EtherCAT register list

(1) Peripheral Function Registers

Register name	Shortcut	bits	Address[NOTE]
EtherCAT PHY offset address setting	CATOFFADD	32	BASE+0620H
EtherCAT operation mode setting	CATEMMD	32	BASE+0624H
EtherCAT reset	CATRESET	32	BASE+0628H

(2) ESC Information Registers

Register name	Shortcut	bits	Address
Type	TYPE	8	400E 0000H
Revision	REVISION	8	400E 0001H
Build	BUILD	16	400E 0002H
FMMUs supported	FMMU_NUM	8	400E 0004H
SyncManagers supported	SYNC_MANAGER	8	400E 0005H
RAM Size	RAM_SIZE	8	400E 0006H
Port Descriptor	PORT_DESC	8	400E 0007H
ESC Features supported	FEATURE	16	400E 0008H

(3) Station Address Registers

Register name	Shortcut	bits	Address
Configured Station Address	STATION_ADR	16	400E 0010H
Configured Station Alias	STATION_ALIAS	16	400E 0012H

(4) Write Protection Registers

Register name	Shortcut	bits	Address
Write Register Enable	WR_REG_ENABLE	8	400E 0020H
Write Register Protection	WR_REG_PROTECT	8	400E 0021H
ESC Write Enable	ESC_WR_ENABLE	8	400E 0030H
ESC Write Protection	ESC_WR_PROTECT	8	400E 0031H

(5) Data Link Layer Registers

Register name	Shortcut	bits	Address
ESC Reset ECAT	ESC_RESET_ECAT	8	400E 0040H
ESC Reset PDI	ESC_RESET_PDI	8	400E 0041H
ESC DL Control	ESC_DL_CONTROL	32	400E 0100H
Physical Read/Write Offset	PHYSICAL_RW_OFFSET	16	400E 0108H
ESC DL Status	ESC_DL_STATUS	16	400E 0110H

(6) Application Layer Registers

Register name	Shortcut	bits	Address
AL Control	AL_CONTROL	16	400E 0120H
AL Status	AL_STATUS	16	400E 0130H
AL Status Code	AL_STATUS_CODE	16	400E 0134H
RUN LED Override	RUN_LED_OVERRIDE	8	400E 0138H
ERR LED Override	ERR_LED_OVERRIDE	8	400E 0139H

(7) PDI Registers

Register name	Shortcut	bits	Address
PDI Control	PDI_CONTROL	8	400E 0140H
ESC Configuration	ESC_CONFIG	8	400E 0141H
PDI Configuration	PDI_CONFIG	8	400E 0150H
SYNC/LATCH PDI Configuration	SYNC_LATCH_CONFIG	16	400E 0151H
Extended PDI Configuration	EXT_PDI_CONFIG	16	400E 0152H

(8) Interrupts Registers

Register name	Shortcut	bits	Address
ECAT Event Mask	ECAT_EVENT_MASK	16	400E 0200H
AL Event Mask	AL_EVENT_MASK	32	400E 0204H
ECAT Event Request	ECAT_EVENT_REQ	16	400E 0210H
AL Event Request	AL_EVENT_REQ	32	400E 0220H

(9) Error Counters Registers (n=0..1)

Register name	Shortcut	bits	Address
Rx Error Counter n	RX_ERR_COUNTn	16	400E 0300H + 0002H*n
Forwarded Rx Error counter n	FWD_RX_ERR_COUNTn	8	400E 0308H + 0001H*n
ECAT Processing Unit Error Counter	ECAT_PROC_ERR_COUNT	8	400E 030CH
PDI Error Counter	PDI_ERR_COUNT	8	400E 030DH
Lost Link Counter n	LOST_LINK_COUNTn	8	400E 0310H + 0001H*n

(10) Watchdog Registers

Register name	Shortcut	bits	Address
Watchdog Divider	WD_DIVIDE	16	400E 0400H
Watchdog Time PDI	WDT_PDI	16	400E 0410H
Watchdog Time Process Data	WDT_DATA	16	400E 0420H
Watchdog Status Process Data	WDS_DATA	16	400E 0440H
Watchdog Counter Process Data	WDC_DATA	8	400E 0442H
Watchdog Counter PDI	WDC_PDI	8	400E 0443H

(11) SII EEPROM Interface Registers

Register name	Shortcut	bits	Address
EEPROM Configuration	EEP_CONF	8	400E 0500H
EEPROM PDI Access State	EEP_STATE	8	400E 0501H
EEPROM Control/Status	EEP_CONT_STAT	16	400E 0502H
EEPROM Address	EEP_ADR	32	400E 0504H
EEPROM Data	EEP_DATA	32	400E 0508H

(12) MII Management Interface Registers (n=0..1)

Register name	Shortcut	bits	Address
MII Management Control/Status	MII_CONT_STAT	16	400E 0510H
PHY Address	PHY_ADR	8	400E 0512H
PHY Register Address	PHY_REG_ADR	8	400E 0513H
PHY Data	PHY_DATA	16	400E 0514H
MII Management ECAT Access State	MII_ECAT_ACS_STAT	8	400E 0516H
MII Management PDI Access State	MII_PDI_ACS_STAT	8	400E 0517H
PHY Port Status n	PHY_STATUSn	8	400E 0518H + 0001H*n

(13) FMMU Registers (m=0..7)

Register name	Shortcut	bits	Address
FMMU Logical Start Address m	FMMUm.L_START_ADR	32	400E 0600H + 0010H*m
FMMU Length m	FMMUm.LEN	16	400E 0604H + 0010H*m
FMMU Logical Start bit m	FMMUm.L_START_BIT	8	400E 0606H + 0010H*m
FMMU Logical Stop bit m	FMMUm.L_STOP_BIT	8	400E 0607H + 0010H*m
FMMU Physical Start Address m	FMMUm.P_START_ADR	16	400E 0608H + 0010H*m
FMMU Physical Start bit m	FMMUm.P_START_BIT	8	400E 060AH + 0010H*m
FMMU Type m	FMMUm.TYPE	8	400E 060BH + 0010H*m
FMMU Activate m	FMMUm.ACT	8	400E 060CH + 0010H*m

(14) SyncManager Registers (m=0..7)

Register name	Shortcut	bits	Address
SyncManager Physical Start Address m	SMm.P_START_ADR	16	400E 0800H + 0008H*m
SyncManager Length m	SMm.LEN	16	400E 0802H + 0008H*m
SyncManager Control m	SMm.CONTROL	8	400E 0804H + 0008H*m
SyncManager Status m	SMm.STATUS	8	400E 0805H + 0008H*m
SyncManager Activate m	SMm.ACT	8	400E 0806H + 0008H*m
SyncManager PDI Control m	SMm.PDI_CONT	8	400E 0807H + 0008H*m

(15) Distributed Clocks Registers

Register name	Shortcut	bits	Address
DC – Receive Times registers			
Receive Times Port0	DC_RCV_TIME_PORT0	32	400E 0900H
Receive Times Port1	DC_RCV_TIME_PORT1	32	400E 0904H
DC – Time Loop Control Unit registers			
System Time	DC_SYS_TIME	64	400E 0910H
Receive Time ECAT Processing Unit	DC_RCV_TIME_UNIT	64	400E 0918H
System Time Offset	DC_SYS_TIME_OFFSET	64	400E 0920H
System Time Delay	DC_SYS_TIME_DELAY	32	400E 0928H
System Time Difference	DC_SYS_TIME_DIFF	32	400E 092CH
Speed Counter Start	DC_SPEED_COUNT_START	16	400E 0930H
Speed Counter Diff	DC_SPEED_COUNT_DIFF	16	400E 0932H
System Time Difference Filter Depth	DC_SYS_TIME_DIFF_FIL_DEPTH	8	400E 0934H
Speed Counter Filter Depth	DC_SPEED_COUNT_FIL_DEPTH	8	400E 0935H
DC – Cyclic Unit Control registers			
Cyclic Unit Control	DC_CYC_CONT	8	400E 0980H
DC – SYNC Out Unit registers			
Activation	DC_ACT	8	400E 0981H
Pulse Length of SyncSignals	DC_PULSE_LEN	16	400E 0982H
Activation Status	DC_ACT_STAT	8	400E 0984H
SYNC0 Status	DC_SYNC0_STAT	8	400E 098EH
SYNC1 Status	DC_SYNC1_STAT	8	400E 098FH
Start Time Cyclic Operation / Next SYNC0 Pulse	DC_CYC_START_TIME	64	400E 0990H
Next SYNC1 Pulse	DC_NEXT_SYNC1_PULSE	64	400E 0998H
SYNC0 Cycle Time	DC_SYNC0_CYC_TIME	32	400E 09A0H
SYNC1 Cycle Time	DC_SYNC1_CYC_TIME	32	400E 09A4H
DC – Latch In Unit registers			
Latch0 Control	DC_LATCH0_CONT	8	400E 09A8H
Latch1 Control	DC_LATCH1_CONT	8	400E 09A9H
Latch0 Status	DC_LATCH0_STAT	8	400E 09AEH
Latch1 Status	DC_LATCH1_STAT	8	400E 09AFH
Latch0 Time Positive Edge	DC_LATCH0_TIME_POS	64	400E 09B0H
Latch0 Time Negative Edge	DC_LATCH0_TIME_NEG	64	400E 09B8H
Latch1 Time Positive Edge	DC_LATCH1_TIME_POS	64	400E 09C0H
Latch1 Time Negative Edge	DC_LATCH1_TIME_NEG	64	400E 09C8H
DC – SyncManager Event Times registers			
Buffer Change Event Time	DC_ECAT_CNG_EV_TIME	32	400E 09F0H
PDI Buffer Start Event Time	DC_PDI_START_EV_TIME	32	400E 09F8H
PDI Buffer Change Event Time	DC_PDI_CNG_EV_TIME	32	400E 09FCH

(16) ETC Registers

Register name	Shortcut	byte	Address
PRODUCT ID	PRODUCT_ID	8	400E 0E00H
Vender ID	VENDOR_ID	8	400E 0E08H
User RAM	USER_RAM	128	400E 0F80H - 400E 0FFFH
Process Data RAM	DATA_RAM	8K	400E 1000H - 400E 2FFFH

Caution 1 When accessing (1) Peripheral function registers via the external microcontroller interface, the base address is D_0000H. When accessing these registers from the CPU or DMA controller, the base address is 4001_0000H.

- When accessing from the CPU or DMA controller

BASE = 4001_0000H

- When accessing via the external microcontroller interface

BASE = D_0000H

2 When accessing via the external microcontroller interface, only User RAM and Process Data RAM (400E 0F80H – 400E 2FFF) can be accessible in the whole ESC memory area (400E 0000H – 400E 2FFFH).

6.6 Peripheral Function Registers

6.6.1 EtherCAT PHY offset address setting register (CATOFFADD)

CATOFFADD register set the offset address of Ether PHY in case of using EtherCAT.
This register can be read/written in 32-bit or 16bit units.

Caution This register can be written only in case of releasing protection by specific sequence using system protects command register (SYSPCMD). Please refer to system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary in case of reading the value of this register. Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of system protect command register (SYSPCMD).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATOFFADD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	OADD4	OADD3	OADD2	OADD1	OADD0	BASE+0620H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	0000 0000H

Bit position	Bit name	Function
4-0	OADD4- OADD0	Set the offset address of PHY of using EtherCAT

6.6.2 EtherCAT operation mode setting register (CATEMMD)

CATEMMD register set the operation mode in case of using EtherCAT.
This register can be read/written in 32-bit or 16bit units.

Caution This register can be written only in case of releasing protection by specific sequence using system protect command register (SYSPCMD). Please refer to system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary in case of reading the value of this register. Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of system protect command register (SYSPCMD).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATEMMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	I2CSIZE	BASE+0624H
																																	Initial Value
																																	0000 0000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	

Bit position	Bit name	Function
0	I2CSIZE	Set the I2C memory size of EtherCAT 0 : 16Kbit or less 1 : 32Kbit to 4Mbit

6.6.3 EtherCAT reset register (CATRESET)

PHYMD register control the reset operation of EtherCAT. EtherCAT is reset status when R-IN32M3 is started.

Please released reset by this register after completion of shared port setting of EtherCAT. In addition, please reset EtherCAT again by this register when the reset interrupt occurs from EtherCAT.

This register can be read/written in 32-bit units.

Caution1. This register can be written only in case of releasing protection by specific sequence using system protect command register (SYSPCMD). Please refer to system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary in case of reading the value of this register. Please refer to "R-IN32M3 User's Manual Peripheral functions edition" for the detail of system protect command register (SYSPCMD).

Caution2. Please release the reset after securing time to satisfy reset width to EtherPHY by software in case of reset ting EtherCAT again.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
CATRESET	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CATRST	BASE+0628H
																																	Initial Value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	0000 0000H

Bit position	Bit name	Function
0	CATRST	Reset EtherCAT 0 : during reset 1 : release reset

6.7 ESC Information Register

6.7.1 Type register (TYPE)

This register indicates the type of the EtherCAT Slave Controller

	7	6	5	4	3	2	1	0	Address	Initial Value
TYPE	TYPE								400E 0000H	A0H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	TYPE	Type of the EtherCAT Slave Controller

6.7.2 Revision register (REVISION)

This register indicates the revision of the EtherCAT Slave Controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
REVISION	REV								400E 0001H	01H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	REV	Revision of the EtherCAT Slave Controller

6.7.3 Build register (BUILD)

This register indicates the build number of the EtherCAT Slave Controller.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
BUILD	BUILD																400E 0002H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	BUILD	Build number of the EtherCAT Slave Controller

6.7.4 FMMUs supported register (FMMU_NUM)

This register indicates the number of supported FMMU channels (or entities) of the EtherCAT Slave Controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMU_NUM	NUMFMMU								400E 0004H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	NUMFMMU	Number of supported FMMU channels (or entities) of the EtherCAT Slave Controller.

6.7.5 SyncManagers supported register (SYNC_MANAGER)

This register indicates the number of supported SyncManager channels (or entities) of the EtherCAT Slave Controller.

	7	6	5	4	3	2	1	0	Address	Initial Value
SYNC_ MANAGER	NUMSYNC								400E 0005H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	NUMSYNC	Number of supported SyncManager channels (or entities) of the EtherCAT Slave Controller

6.7.6 RAM Size register (RAM_SIZE)

This register indicates the Process Data RAM size supported by the EtherCAT Slave Controller in Kbyte.

	7	6	5	4	3	2	1	0	Address	Initial Value
RAM_SIZE	RAMSIZE								400E 0006H	08H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	RAMSIZE	Process Data RAM size supported by the EtherCAT Slave Controller in KByte

6.7.7 Port Descriptor register (PORT_DESC)

This register indicates the port configuration.

	7	6	5	4	3	2	1	0	Address	Initial Value
PORT_DESC	P3		P2		P1		P0		400E 0007H	0FH
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-6	P3	Port3 configuration: This LSI doesn't implement port3. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII
5-4	P2	Port2 configuration: This LSI doesn't implement port2. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII
3-2	P1	Port1 configuration: This LSI is MII. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII
1-0	P0	Port0 configuration: This LSI is MII. 00: Not implemented 01: Not configured (SII EEPROM) 10: EBUS 11: MII / RMII

6.7.8 ESC Features supported register (FEATURE)

This register indicates the features supported by the EtherCAT Slave Controller.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FEATURE	0	0	0	0	FSCONFIG	RWSUPP	LRW	DCSYNC	FCS	LINKDECMII	0	0	DCWID	DC	0	FMMU	400E 0008H	018CH
ECAT	0	0	0	0	R	R	R	R	R	R	0	0	R	R	0	R		
PDI	0	0	0	0	R	R	R	R	R	R	0	0	R	R	0	R		

Bit position	Bit name	Function
11	FSCONFIG	Fixed FMMU/SyncManager configuration 0: Variable configuration 1: Fixed configuration
10	RWSUPP	EtherCAT read/write command support(BRW, APRW, FPRW): 0: Supported 1: Not supported
9	LRW	EtherCAT LRW command support: 0: Supported 1: Not supported
8	DCSYNC	Enhanced DC SYNC Activation 0: Not available 1: Available
7	FCS	Separate Handling of FCS Errors: 0: Not supported 1: Supported, frames with wrong FCS and additional nibble will be counted separately in Forwarded RX Error Counter
6	LINKDECMII	Enhanced Link Detection MII: 0: Not available 1: Available
3	DCWID	Distributed Clocks (width): 0: 32 bit 1: 64 bit
2	DC	Distributed Clocks: 0: Not available 1: Available
0	FMMU	FMMU Operation: 0: Bit oriented 1: Byte oriented

6.8 Station Address Registers

6.8.1 Configured Station Address register (STATION_ADR)

This register indicates the address used for node addressing.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
STATION_ADR	NODADDR																400E 0010H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	NODADDR	Address used for node addressing (FPxx commands)

6.8.2 Configured Station Alias register (STATION_ALIAS)

This register indicates the alias address used for node addressing (FPxx commands).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
STATION_ALIAS	NODALIADDR																400E 0012H	0000H[Note]
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit position	Bit name	Function
15-0	NODALIADDR	Alias Address used for node addressing (FPxx commands). The use of this alias is activated by Register DL Control Bit 24 (0x0100.24/0x0103.0).

Note Initial Value is 0 until first EEPROM load, then EEPROM ADR 0x0004.
EEPROM value is only taken over at first EEPROM load after power-on or reset.

6.9 Write Protection Registers

6.9.1 Write Register Enable register (WR_REG_ENABLE)

This register is used to release the write protection temporarily when Write Register Protection is enabled.

	7	6	5	4	3	2	1	0	Address	Initial Value
WR_REG_ENABLE	0	0	0	0	0	0	0	ENABLE	400E 0020H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	ENABLE	If write register protection is enabled, this register has to be written in the same Ethernet frame (value does not care) before other writes to this station are allowed. Write protection is still active after this frame (if Write Register Protection register is not changed).

6.9.2 Write Register Protection register (WR_REG_PROTECT)

This register is used to protect from writing register. The register in the area 400E 0000H to 400E 0FFFH are write protected (excluding 0x0020 and 0x0030).

	7	6	5	4	3	2	1	0	Address	Initial Value
WR_REG_PROTECT	0	0	0	0	0	0	0	PROTECT	400E 0021H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	PROTECT	Write register protection: 0: Protection disabled 1: Protection enabled Registers 0x0000-0x0F0F are write protected, except for 0x0030.

6.9.3 ESC Write Enable register (ESC_WR_ENABLE)

This register is used to release the write protection temporarily when ESC Write Protection is enabled.

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_WR_ENABLE	0	0	0	0	0	0	0	ENABLE	400E 0030H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	ENABLE	If ESC write protection is enabled, this register has to be written in the same Ethernet frame (value does not care) before other writes to this station are allowed. ESC write protection is still active after this frame(if ESC Write Protection register is not changed).

6.9.4 ESC Write Protection register (ESC_WR_PROTECT)

This register is used to protect from writing register and Process Data RAM. The area 400E 0000H to 400E 2FFFH are write protected (excluding 0x0020 and 0x0030).

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_WR_PROTECT	0	0	0	0	0	0	0	PROTECT	400E 0031H	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	PROTECT	Write protect: 0: Protection disabled 1: Protection enabled All areas are write protected, except for 0x0030.

6.10 Data Link Layer Registers

6.10.1 ESC Reset ECAT register (ESC_RESET_ECAT)

This register is used to reset the EtherCAT Slave Controller from ECAT(master) by software.

Write:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_ECAT	RESET_ECAT								400E 0040H	00H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	RESET_ECAT	A reset is asserted after writing 0x52 ("R"), 0x45 ("E") and 0x53 ("S") in this register with 3 consecutive frames.

Read:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_ECAT	0	0	0	0	0	0	RESET_ECAT		400E 0040H	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit position	Bit name	Function
1-0	RESET_ECAT	Progress of the reset procedure: 01: after writing 0x52 10: after writing 0x45 (if 0x52 was written before) 00: else

6.10.2 ESC Reset PDI register (ESC_RESET_PDI)

This register is used to reset the EtherCAT Slave Controller from PDI(slave) by software.

Write:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_PDI	RESET_PDI								400E 0041H	00H
ECAT	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit position	Bit name	Function
7-0	RESET_PDI	A reset is asserted after writing 0x52 ("R"), 0x45 ("E") and 0x53 ("S") in this register with 3 consecutive frames.

Read:

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_RESET_PDI	0	0	0	0	0	0	RESET_PDI		400E 0041H	00H
ECAT	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	R/W	R/W		

Bit position	Bit name	Function
1-0	RESET_PDI	Progress of the reset procedure: 01: after writing 0x52 10: after writing 0x45 (if 0x52 was written before) 00: else

6.10.3 ESC DL Control register (ESC_DL_CONTROL)

This register is used to control loop and configure RX FIFO size and Station Alias.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
ESC_DL_CONTROL	0	0	0	0	0	0	0	STAALIAS	0	0	0	0	0	RXFIFO			LP3		LP2		LP1		LP0		0	0	0	0	0	0	TEMPUSE	FWDRULE	400E 0100H
																																	Initial Value
																																	0007 C001H
ECAT	0	0	0	0	0	0	0	R/W	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	0	R/W	R/W	
PDI	0	0	0	0	0	0	0	R	0	0	0	0	0	R	R	R	R	R	R	R	R	R	R	R	0	0	0	0	0	0	R	R	

Bit position	Bit name	Function
24	STAALIAS	Station alias: 0: Ignore Station Alias 1: Alias can be used for all configured address command types (FPRD, FPWR, …)
18-16	RXFIFO	RX FIFO Size (ESC delays start of forwarding until FIFO is at least half full). RX FIFO Size : RX delay reduction 0-3: -40 ns 4-6: no change 7: default
15-14	LP3	Loop Port 3: (Port3 is not available on this LSI.) 00: Auto 01: Auto Close 10: Open 11: Closed
13-12	LP2	Loop Port 2: (Port2 is not available on this LSI.) 00: Auto 01: Auto Close 10: Open 11: Closed
11-10	LP1	Loop Port 1: 00: Auto 01: Auto Close 10: Open 11: Closed
9-8	LP0	Loop Port 0: 00: Auto 01: Auto Close 10: Open 11: Closed
1	TEMPUSE	Temporary use of settings in Register 0x101: 0: permanent use 1: use for about 1 second, then revert to previous settings
0	FWDRULE	Forwarding rule: 0: EtherCAT frames are processed, Non-EtherCAT frames are forwarded without processing. 1: EtherCAT frames are processed, Non-EtherCAT frames are destroyed. The source MAC address is changed for every frame (SOURCE_MAC[1] is set to 1 –locally administered address) regardless of the forwarding rule.

Caution 1 Loop configuration changes are delayed until the end of a currently received or transmitted frame at the port.

2 The possibility of RX FIFO Size reduction depends on the clock source accuracy of the ESC and of every connected EtherCAT/Ethernet devices (master, slave, etc.). RX FIFO Size of 7 is sufficient for 100ppm accuracy, FIFO Size 0 is possible with 25ppm accuracy (frame size of 1518/1522 Byte).

6.10.4 Physical Read/Write Offset register (PHYSICAL_RW_OFFSET)

This register is used to set offset size between read address and write address in the R/W command.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
PHYSICAL_RW_OFFSET	RWOFFSET																400E 0108H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	RWOFFSET	Offset of R/W Commands (FPRW, APRW) between Read address and Write address. RD_ADR = ADR and WR_ADR = ADR +R/W-Offset

6.10.5 ESC DL Status register (ESC_DL_STATUS)

This register indicates EtherCAT Slave Controller status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_DL_STATUS	COMP3	LP3	COMP2	LP2	COMP1	LP1	COMP0	LP0	PHYP3	PHYP2	PHYP1	PHYP0	0	ENHLINKD	PDIWDST	PDIOPE	400E 0110H	0004H
ECAT	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)	0	R (ack)	R (ack)	R (ack)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	0	R	R	R		

Bit position	Bit name	Function
15	COMP3	Communication on Port 3: (Port 3 is not available on this LSI.) 0: No stable communication 1: Communication established
14	LP3	Loop Port 3: (Port 3 is not available on this LSI.) 0: Open 1: Closed
13	COMP2	Communication on Port 2: (Port 2 is not available on this LSI.) 0: No stable communication 1: Communication established
12	LP2	Loop Port 2: (Port 2 is not available on this LSI.) 0: Open 1: Closed
11	COMP1	Communication on Port 1: 0: No stable communication 1: Communication established
10	LP1	Loop Port 1: 0: Open 1: Closed
9	COMP0	Communication on Port 0: 0: No stable communication 1: Communication established
8	LP0	Loop Port 0: 0: Open 1: Closed
7	PHYP3	Physical link on Port 3: (Port 3 is not available on this LSI.) 0: No link 1: Link detected
6	PHYP2	Physical link on Port 2: (Port 2 is not available on this LSI.) 0: No link 1: Link detected
5	PHYP1	Physical link on Port 1: 0: No link 1: Link detected
4	PHYP0	Physical link on Port 0: 0: No link 1: Link detected

2	ENHLINKD	Enhanced Link detection: 0: Deactivated for all ports 1: Activated for at least one port NOTE: EEPROM value is only taken over at first EEPROM load after power-on or reset
1	PDIWDST	PDI Watchdog Status: 0: Watchdog expired 1: Watchdog reloaded
0	PDIOPE	PDI operational/EEPROM loaded correctly: 0: EEPROM not loaded, PDI not operational (no access to Process Data RAM) 1: EEPROM loaded correctly, PDI operational (access to Process Data RAM)

Note Reading DL Status register from ECAT clears ECAT Event Request 0x0210[2].

6.11 Application Layer Registers

6.11.1 AL Control register (AL_CONTROL)

This register is used to initiate State Transition of the Device State Machine and to acknowledge error indication.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_CONTROL	0	0	0	0	0	0	0	0	0	0	0	ERRINDACK	INISTATE				400E 0120H	0001H
ECAT	0	0	0	0	0	0	0	0	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	0	0	0	0	0	R/ (clear)	R/ (clear)	R/ (clear)	R/ (clear)	R/ (clear)		

Bit position	Bit name	Function
4	ERRINDACK	Error Ind Ack: 0: No Ack of Error Ind in AL status register 1: Ack of Error Ind in AL status register
3-0	INISTATE	Initiate State Transition of the Device State Machine: 1: Request Init State 3: Request Bootstrap State 2: Request Pre-Operational State 4: Request Safe-Operational State 8: Request Operational State

Note The PDI has to read the AL Control register after ECAT has written it. Otherwise ECAT can not write again to the AL Control register. After Reset, AL Control register can be written by ECAT. (Regarding mailbox functionality, both registers 0x0120 and 0x0121 are equivalent, e.g. reading 0x0121 is sufficient to make this register writeable again.)
Reading AL Control from PDI clears AL Event Request 0x0220[0].

6.11.2 AL Status register (AL_STATUS)

This register indicates Slave application status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_STATUS	0	0	0	0	0	0	0	0	0	0	0	ERR	ACTSTATE				400E 0130H	0001H
ECAT	0	0	0	0	0	0	0	0	0	0	0	R (ack)	R (ack)	R (ack)	R (ack)	R (ack)		
PDI	0	0	0	0	0	0	0	0	0	0	0	R/(w)	R/(w)	R/(w)	R/(w)	R/(w)		

Bit position	Bit name	Function
4	ERR	Error Ind: 0: Device is in State as requested or Flag cleared by command 1: Device has not entered requested State or changed State as result of a local action
3-0	ACTSTATE	Actual State of the Device State Machine: 1: Init State 3: Request Bootstrap State 2: Pre-Operational State 4: Safe-Operational State 8: Operational State

Note Reading AL Status register from ECAT clears ECAT Event Request 0x0210[3].

6.11.3 AL Status Code register (AL_STATUS_CODE)

This register indicates error code from slave application.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
AL_STATUS_CODE	STATUSCODE																400E 0134H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		

Bit position	Bit name	Function
15-0	STATUSCODE	AL Status Code. Error codes from the slave application.

6.11.4 RUN LED Override register (RUN_LED_OVERRIDE)

This register is used to override RUN LED control.

	7	6	5	4	3	2	1	0	Address	Initial Value
RUN_LED_OVERRIDE	0	0	0	OVERRIDEEN	LEDCODE				400E 0138H	00H
ECAT	0	0	0	R/W	R/W	R/W	R/W	R/W		
PDI	0	0	0	R/W	R/W	R/W	R/W	R/W		

Bit position	Bit name	Function
4	OVERRIDEEN	Enable Override: 0: Override disabled 1: Override enabled
3-0	LEDCODE	LED code: (FSM State:) 0x0: Off (1-Init) 0x1-0xC: Flash 1x – 12x (4-SafeOp 1x) 0xD: Blinking (2-PreOp) 0xE: Flickering (3-Bootrap) 0xF: On (8-Op)

Caution Changes to AL Status register (0x0130) with valid values will disable RUN LED Override (0x0138[4]=0). The value read in this register always reflects current LED output.
Normally RUN LED is controlled by AL Status register automatically. It is not necessary to override RUN LED in order to indicate status of general state machine.
E.g. it is available to use this register in order to indicate specific slave position.

6.11.5 ERR LED Override register (ERR_LED_OVERRIDE)

This register is used to override ERR LED control.

	7	6	5	4	3	2	1	0	Address	Initial Value
ERR_LED_OVERRIDE	0	0	0	OVERRIDEEN	LEDCODE				400E 0139H	00H
ECAT	0	0	0	R/W	R/W	R/W	R/W	R/W		
PDI	0	0	0	R/W	R/W	R/W	R/W	R/W		

Bit position	Bit name	Function
4	OVERRIDEEN	Enable Override: 0: Override disabled 1: Override enabled
3-0	LEDCODE	LED code: 0x0: Off 0x1-0xC: Flash 1x – 12x 0xD: Blinking 0xE: Flickering 0xF: On

Caution New error conditions will disable ERR LED Override (0x0139[4]=0). The value read in this register always reflects current LED output.
ESC automatically controls ERR LED in the condition below,
SII EEPROM load error
PDI watchdog timeout
Regarding the other errors, ERR LED should be controlled by application using this register.

6.12 PDI Registers

6.12.1 PDI Control register (PDI_CONTROL)

This register indicates the type of PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_CONTROL	PDI								400E 0140H	80H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	PDI	Process data interface: This LSI indicates the below value. 0x80: On-chip bus

6.12.2 ESC Configuration register (ESC_CONFIG)

This register indicates ESC configuration.

	7	6	5	4	3	2	1	0	Address	Initial Value
ESC_CONFIG	ENLP3	ENLP2	ENLP1	ENLP0	DCLATCH	DCSYNC	ENLALLP	DEVEMU	400E 0141H	0CH
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7	ENLP3	Enhanced Link port 3: (Port3 is not available on this LSI.) 0: disabled (if bit 9=0) 1: enabled
6	ENLP2	Enhanced Link port 2: (Port2 is not available on this LSI.) 0: disabled (if bit 9=0) 1: enabled
5	ENLP1	Enhanced Link port 1: 0: disabled (if bit 9=0) 1: enabled
4	ENLP0	Enhanced Link port 0: 0: disabled (if bit 9=0) 1: enabled
3	DCLATCH	Distributed Clocks Latch In Unit: (Fixed to 1 in this LSI). 0: disabled (power saving) 1: enabled
2	DCSYNC	Distributed Clocks SYNC Out Unit: (Fixed to 1 in this LSI) 0: disabled (power saving) 1: enabled
1	ENLALLP	Enhanced Link detection all ports: 0: disabled (if bits [15:12]=0) 1: enabled at all ports
0	DEVEMU	Device emulation (control of AL status): 0: AL status register has to be set by PDI 1: AL status register will be set to value written to AL control register

6.12.3 PDI Configuration register (PDI_CONFIG)

This register indicates PDI configuration.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_CONFIG	ONCHIPBUS			ONCHIPBUSCLK					400E 0150H	44H
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-5	ONCHIPBUS	On-chip bus type: This LSI indicates 010.
4-0	ONCHIPBUSCLK	On-chip bus clock: This LSI indicates 4 (100MHz).

6.12.4 SYNC/LATCH PDI Configuration register (SYNC_LATCH_CONFIG)

This register indicates the configuration of SYNC output and LATCH input.

	7	6	5	4	3	2	1	0	Address	Initial Value
SYNC_LATCH_CONFIG	SYNC1MAP	SYNCLAT1	SYNC1OUT		SYNC0MAP	SYNCLAT0	SYNC0OUT		400E 0151H	EEH
ECAT	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7	SYNC1MAP	SYNC1 mapped to AL Event Request register 0x0220.3: (This LSI always indicates 1) 0: Disabled 1: Enabled
6	SYNCLAT1	SYNC1/LATCH1 configuration: (This LSI always indicates 1)[Caution] 0: LATCH1 input 1: SYNC1 output
5-4	SYNC1OUT	SYNC1 output driver/polarity:This LSI always indicates 10 (Push-Pull active high.
3	SYNC0MAP	SYNC0 mapped to AL Event Request register 0x0220.2: (This LSI always indicates 1) 0: Disabled 1: Enabled
2	SYNCLAT0	SYNC0/LATCH0 configuration: (This LSI always indicates 1) [Caution] 0: LATCH0 input 1: SYNC0 output
1-0	SYNC0OUT	SYNC0 output driver/polarity:This LSI always indicates 10 (Push-Pull active high.

Caution Latch input is available though value indicates SYNC output. Use chip level pin multiplex function in order to switch SYNC output to LATCH input and versa vice.

6.12.5 Extended PDI Configuration register (EXT_PDI_CONFIG)

This register indicates extended PDI configuration.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
EXT_PDI_CONFIG	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DATABUSWID		400E 0152H	00H
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R		

Bit position	Bit name	Function
1-0	DATABUSWID	Data Bus Width W: (This LSI indicates 0 (4 Byte).) 0: 4 Byte 1: 1 Byte 2: 2 Byte 3: Reserved

6.13 Interrupts Registers

6.13.1 ECAT Event Mask register (ECAT_EVENT_MASK)

ECAT event request (ECAT interrupt) is used to transmit the slave event to EtherCAT master. This register is used to set mask to each event of ECAT event request register. This register and ECAT event request register are ANDed and it is used as interrupt.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_EVENT_MASK	ECATEVMASK																400E 0200H	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	ECATEVMASK	ECAT Event masking of the ECAT Event Request Events for mapping into ECAT event field of EtherCAT frames: 0: Corresponding ECAT Event Request register bit is not mapped 1: Corresponding ECAT Event Request register bit is mapped

6.13.2 AL Event Mask register (AL_EVENT_MASK)

AL event request (PDI interrupt) is used to transmit the ESC interrupt to the slave application. This register is used to set mask to each event of AL event request register. This register and AL event request register are ANDed and it is used as interrupt.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
AL_EVENT_MASK	ALEVMASK																																400E 0204H Initial Value 00FF FF0FH
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
PDI	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit position	Bit name	Function
31-0	ALEVMASK	AL Event masking of the AL Event Request register Events for mapping to PDI IRQ signal: 0: Corresponding AL Event Request register bit is not mapped 1: Corresponding AL Event Request register bit is mapped

6.13.3 ECAT Event Request register (ECAT_EVENT_REQ)

This register indicates events of ECAT event request (ECAT interrupt).

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_EVENT_REQ	0	0	0	0	SMSTA7	SMSTA6	SMSTA5	SMSTA4	SMSTA3	SMSTA2	SMSTA1	SMSTA0	ALSTA	DLSTA	0	DCLATCH	400E 0210H	0000H
ECAT	0	0	0	0	R	R	R	R	R	R	R	R	R	R	0	R		
PDI	0	0	0	0	R	R	R	R	R	R	R	R	R	R	0	R		

Bit position	Bit name	Function
11	SMSTA7	Mirrors values of SyncManager7 Status: 0: No Sync Channel 7 event 1: Sync Channel 7 event pending
10	SMSTA6	Mirrors values of SyncManager6 Status: 0: No Sync Channel 6 event 1: Sync Channel 6 event pending
9	SMSTA5	Mirrors values of SyncManager5 Status: 0: No Sync Channel 5 event 1: Sync Channel 5 event pending
8	SMSTA4	Mirrors values of SyncManager4 Status: 0: No Sync Channel 4 event 1: Sync Channel 4 event pending
7	SMSTA3	Mirrors values of SyncManager3 Status: 0: No Sync Channel 3 event 1: Sync Channel 3 event pending
6	SMSTA2	Mirrors values of SyncManager2 Status: 0: No Sync Channel 2 event 1: Sync Channel 2 event pending
5	SMSTA1	Mirrors values of SyncManager1 Status: 0: No Sync Channel 1 event 1: Sync Channel 1 event pending
4	SMSTA0	Mirrors values of SyncManager0 Status: 0: No Sync Channel 0 event 1: Sync Channel 0 event pending
3	ALSTA	AL Status event: 0: No change in AL Status 1: AL Status change (Bit is cleared by reading out AL Status0x0130:0x0131 from ECAT)
2	DLSTA	DL Status event: 0: No change in DL Status 1: DL Status change (Bit is cleared by reading out DL Status 0x0110:0x0111 from ECAT)
0	DCLATCH	DC Latch event: 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs (Bit is cleared by reading DC Latch event times from ECAT for ECAT controlled Latch Units, so that Latch 0/1 Status 0x09AE:0x09AF indicates no event)

6.13.4 AL Event Request register (AL_EVENT_REQ)

This register indicates events of AL event request (PDI interrupt).

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
AL_EVENT_REQ	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SMINT7	SMNT6	SMINT5	SMINT4	SMINT3	SMINT2	SMINT1	SMINT0	0	WDPD	0	SYNCACT	DCSYNC1STA	DCSYNC0STA	DCLATCH	ALCTRL	400E 0220H
																																	Initial Value
																																	0000 0000H
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R	R	R	0	R	R	R	R	R	R	R	
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	R	R	R	R	R	R	0	R	R	R	R	R	R	R	

Bit position	Bit name	Function
15	SMINT7	SyncManager 7 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 7 interrupt 1: SyncManager 7 interrupt pending
14	SMINT6	SyncManager 6 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 6 interrupt 1: SyncManager 6 interrupt pending
13	SMINT5	SyncManager 5 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 5 interrupt 1: SyncManager 5 interrupt pending
12	SMINT4	SyncManager 4 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 4 interrupt 1: SyncManager 4 interrupt pending
11	SMINT3	SyncManager 3 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 3 interrupt 1: SyncManager 3 interrupt pending
10	SMINT2	SyncManager 2 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 2 interrupt 1: SyncManager 2 interrupt pending
9	SMINT1	SyncManager 1 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 1 interrupt 1: SyncManager 1 interrupt pending
8	SMINT0	SyncManager 0 interrupts (SyncManager register offset 0x5, bit [0] or [1]): 0: No SyncManager 0 interrupt 1: SyncManager 0 interrupt pending
6	WDPD	Watchdog Process Data: 0: Has not expired 1: Has expired (Bit is cleared by reading Watchdog Status Process Data 0x0440 from PDI)
4	SYNCACT	SyncManager activation register (SyncManager register offset 0x6) changed: 0: No change in any SyncManager 1: At least one SyncManager changed (Bit is cleared by reading SyncManager Activation registers 0x0806 etc. from PDI)
3	DCSYNC1STA	State of DC SYNC1 (if register 0x0151.7=1) (Bit is cleared by reading of SYNC1 status 0x098F from PDI)
2	DCSYNC0STA	State of DC SYNC0 (if register 0x0151.3=1) (Bit is cleared by reading SYNC0 status 0x098E from PDI)
1	DCLATCH	DC Latch event: 0: No change on DC Latch Inputs 1: At least one change on DC Latch Inputs (Bit is cleared by reading DC Latch event times from PDI for PDI controlled Latch Units so that Latch 0/1 Status 0x09AE:0x09AF indicates no event)
0	ALCTRL	AL Control event: 0: No AL Control Register change 1: AL Control Register has been written (Bit is cleared by reading AL Control register 0x0120:0x0121 from PDI)

6.14 Error Counters Registers

6.14.1 Rx Error Counter n register (RX_ERR_COUNTn)

This register counts RX frame errors.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
RX_ERR_ COUNTn	RXERRCNT								INVFRMCNT								400E 0300H + 0002H*n	0000H
ECAT	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)	R/W (clr)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-8	RXERRCNT	RX Error counter of Port n (counting is stopped when 0xFF is reached). This is coupled directly to RX ERR of MII interface. Cleared if one of the RX Error counters 0x0300-0x030B is written.
7-0	INVFRMCNT	Invalid frame counter of Port n (counting is stopped when 0xFF is reached). Cleared if one of the RX Error counters 0x0300-0x030B is written.

Note 1 n=0-1

n=0 : Port 0, n=1 : Port 1

2 The invalid frame counters are incremented if there is an error in the frame format (Preamble, SFD – Start of Frame Delimiter, FCS – Checksum, invalid length). If the FCS is invalid and an additional nibble is appended, the FCS error is not counted. This is why EtherCAT forwards frames with errors with an invalid FCS and an additional nibble.

RX Errors may appear either inside or outside frames. RX Errors inside frames will lead to invalid frames.

6.14.2 Forwarded Rx Error counter n register (FWD_RX_ERR_COUNTn)

This register counts forwarded RX frames errors.

	7	6	5	4	3	2	1	0	Address	Initial Value
FWD_RX_ ERR_COUNTn	FWDERRCNT								400E 0308H + 0001H*n	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	FWDERRCNT	Forwarded error counter of Port n (counting is stopped when 0xFF is reached). Cleared if one of the RX Error counters 0x0300-0x030B is written.

Note n=0-1

n=0 : Port 0, n=1 : Port 1

6.14.3 ECAT Processing Unit Error Counter register (ECAT_PROC_ERR_COUNT)

This register counts error frame errors passing ECAT Processing Unit.

	7	6	5	4	3	2	1	0	Address	Initial Value
ECAT_PROC_ ERR_COUNT	EPUERRCNT								400E 030CH	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	EPUERRCNT	ECAT Processing Unit error counter (counting is stopped when 0xFF is reached). Counts errors of frames passing the Processing Unit (e.g., FCS is wrong or datagram structure is wrong). Cleared if register is written.

6.14.4 PDI Error Counter register (PDI_ERR_COUNT)

This register counts PDI access errors.

	7	6	5	4	3	2	1	0	Address	Initial Value
PDI_ERR_COUNT	PDIERRCNT								400E 030DH	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	PDIERRCNT	PDI Error counter (counting is stopped when 0xFF is reached). Counts if a PDI access has an interface error. Cleared if register is written.

6.14.5 Lost Link Counter n register (LOST_LINK_COUNTn)

This register counts lost links at port n.

	7	6	5	4	3	2	1	0	Address	Initial Value
LOST_LINK_COUNTn	LOSTLINKCNT								400E 0310H + 0001H*n	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	LOSTLINKCNT	Lost Link counter of Port n (counting is stopped when 0xff is reached). Counts only if port loop is Auto or Auto-Close. Only lost links at open ports are counted. Cleared if one of the Lost Link counter registers is written.

Note Only lost links at open ports are counted.

6.15 Watchdogs Registers

6.15.1 Watchdog Divider register (WD_DIVIDE)

This register is used to set the divider ratio for 25MHz as the basic watchdog increment.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WD_DIVIDE	WDDIV																400E 0400H	09C2H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	WDDIV	Watchdog divider: Number of 25 MHz tics (minus 2) that represents the basic watchdog increment. (Default value is 100µs = 2498)

6.15.2 Watchdog Time PDI register (WDT_PDI)

This register is used to set overflow time of PDI watchdog.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDT_PDI	WDTIMPDI																400E 0410H	03E8H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	WDTIMPDI	Watchdog Time PDI: number or basic watchdog increments (Default value with Watchdog divider 100µs means 100ms Watchdog) Watchdog is disabled if Watchdog time is set to 0x0000. Watchdog is restarted with every PDI access

6.15.3 Watchdog Time Process Data register (WDT_DATA)

This register is used to set overflow time of PDI watchdog.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDT_DATA	WDTIMPD																400E 0420H	03E8H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	WDTIMPD	Watchdog Time Process Data: number of basic watchdog increments (Default value with Watchdog divider 100µs means 100ms Watchdog) There is one Watchdog for all SyncManagers. Watchdog is disabled if Watchdog time is set to 0x0000. Watchdog is restarted with every write access to SyncManagers with Watchdog Trigger Enable Bit set.

6.15.4 Watchdog Status Process Data register (WDS_DATA)

This register indicates watchdog status of process data.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
WDS_DATA	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	WDSTAPD	400E 0440H	0000H
ECAT	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R (ack)		

Bit position	Bit name	Function
0	WDSTAPD	Watchdog Status of Process Data (triggered by SyncManagers) 0: Watchdog Process Data expired 1: Watchdog Process Data is active or disabled Reading this register clears AL Event Request 0x0220[6].

6.15.5 Watchdog Counter Process Data register (WDC_DATA)

This register counts Process data watchdog timeout.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDC_DATA	WDCNTPD								400E 0442H	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	WDCNTPD	Watchdog Counter Process Data (counting is stopped when 0xFF is reached). Counts if Process Data Watchdog expires. Cleared if one of the Watchdog counters 0x0442:0x0443 is written.

6.15.6 Watchdog Counter PDI register (WDC_PDI)

This register counts PDI watchdog timeout.

	7	6	5	4	3	2	1	0	Address	Initial Value
WDC_PDI	WDCNTPDI								400E 0443H	00H
ECAT	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)	R/W(clr)		
PDI	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
7-0	WDCNTPDI	Watchdog PDI counter (counting is stopped when 0xFF is reached). Counts if PDI Watchdog expires. Cleared if one of the Watchdog counters 0x0442:0x0443 is written.

6.16 SII EEPROM Interface Registers

EtherCAT controls the SII EEPROM interface if EEPROM configuration register 0x0500.0=0 and EEPROM PDI Access register 0x0501.0=0, otherwise PDI controls the EEPROM interface.

6.16.1 EEPROM Configuration register (EEP_CONF)

This register is used to configure EEPROM access.

	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_CONF	0	0	0	0	0	0	FORCEECAT	CTRLPDI	400E 0500H	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit position	Bit name	Function
1	FORCEECAT	Force ECAT access: 0: Do not change Bit 0x0501.0 1: Reset Bit 0x0501.0 to 0
0	CTRLPDI	EEPROM control is offered to PDI: 0: no 1: yes (PDI has EEPROM control)

6.16.2 EEPROM PDI Access State register (EEP_STATE)

This register is used to configure EEPROM access from PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_STATE	0	0	0	0	0	0	0	PDIACCESS	400E 0501H	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R/(W)		

Bit position	Bit name	Function
0	PDIACCEES	Access to EEPROM: 0: PDI releases EEPROM access 1: PDI takes EEPROM access (PDI has EEPROM control)

6.16.3 EEPROM Control/Status register (EEP_CONT_STAT)

This register is used to control EEPROM access and indicate the status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
EEP_CONT_STAT	BUSY	WRENERR	ACKCMDERR	LOADSTA	CKSUMERR	COMMAND			PROMSIZE	READBYTE	0	0	0	0	0	ECATWREN	400E 0502H	0000H
ECAT	R	R	R	R	R	R/(W)	R/(W)	R/(W)	0	0	0	0	0	0	0	R/(W)		
PDI	R	R	R	R	R	R/(W)	R/(W)	R/(W)	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
15	BUSY	Busy: 0: EEPROM Interface is idle 1: EEPROM Interface is busy
14	WRENERR	Error Write Enable[Caution1]: 0: No error 1: Write Command without Write enable
13	ACKCMDERR	Error Acknowledge/Command [Caution1]: 0: No error 1: Missing EEPROM acknowledge or invalid command
12	LOADSTA	EEPROM loading status: 0: EEPROM loaded, device information ok 1: EEPROM not loaded, device information not available (EEPROM loading in progress or finished with a failure)
11	CKSUMERR	Checksum Error at in ESC Configuration Area: 0: Checksum ok 1: Checksum error
10-8	COMMAND	Command register[Caution2]: Write: Initiate command. Read: Currently executed command Commands: 000: No command/EEPROM idle (clear error bits) 001: Read 010: Write 100: Reload Others: Reserved/invalid commands (do not issue)
7	PROMSIZE	Selected EEPROM Algorithm: 0: 1 address byte (1KBit – 16KBit EEPROMs) 1: 2 address bytes (32KBit – 4 MBit EEPROMs)
6	READBYTE	Supported number of EEPROM read bytes: 0: 4 Bytes 1: 8 Bytes
0	ECATWREN	ECAT write enable[Caution2]: 0: Write requests are disabled 1: Write requests are enabled This bit is always 1 if PDI has EEPROM control.

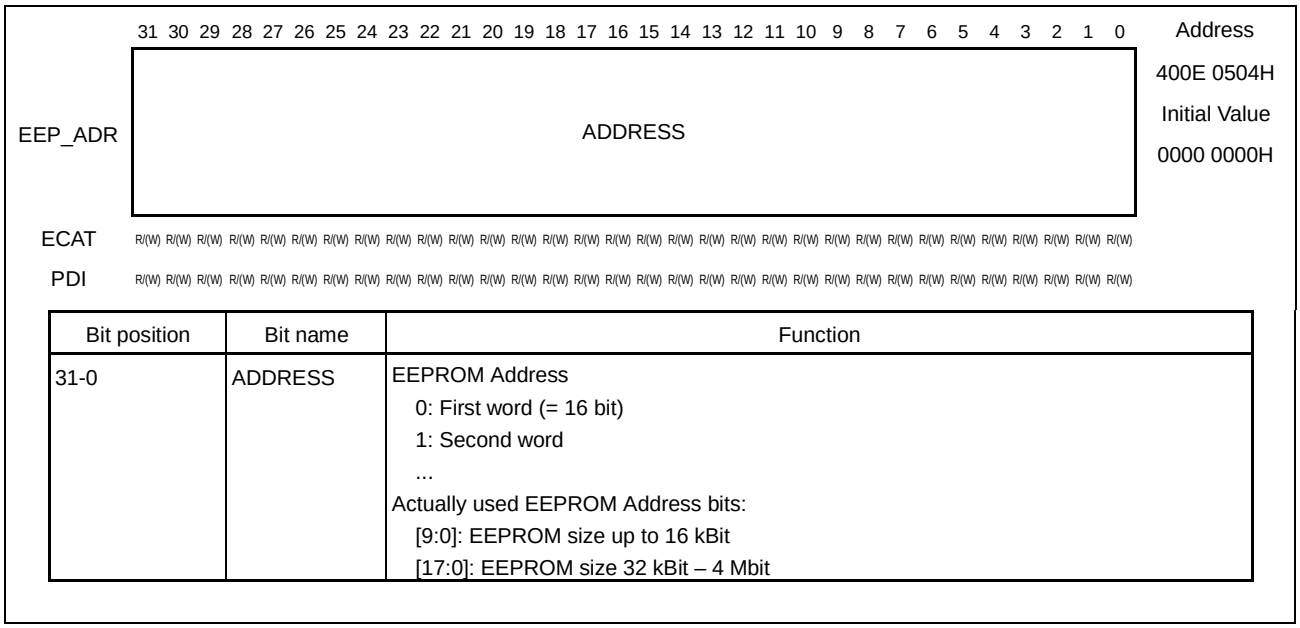
Note Write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if EEPROM interface is busy (0x0502.15=1).

Caution 1 Error bits are cleared by writing "000" (or any valid command) to Command Register Bits [10:8].

2 Write Enable bit 0 is self-clearing at the SOF of the next frame, Command bits [10:8] are self-clearing after the command is executed (EEPROM Busy ends). Writing "000" to the command register will also clear the error bits [14:13]. Command bits [10:8] are ignored if Error Acknowledge/Command is pending (bit 13).

6.16.4 EEPROM Address register (EEP_ADR)

This register is used to set EEPROM address to be accessed.

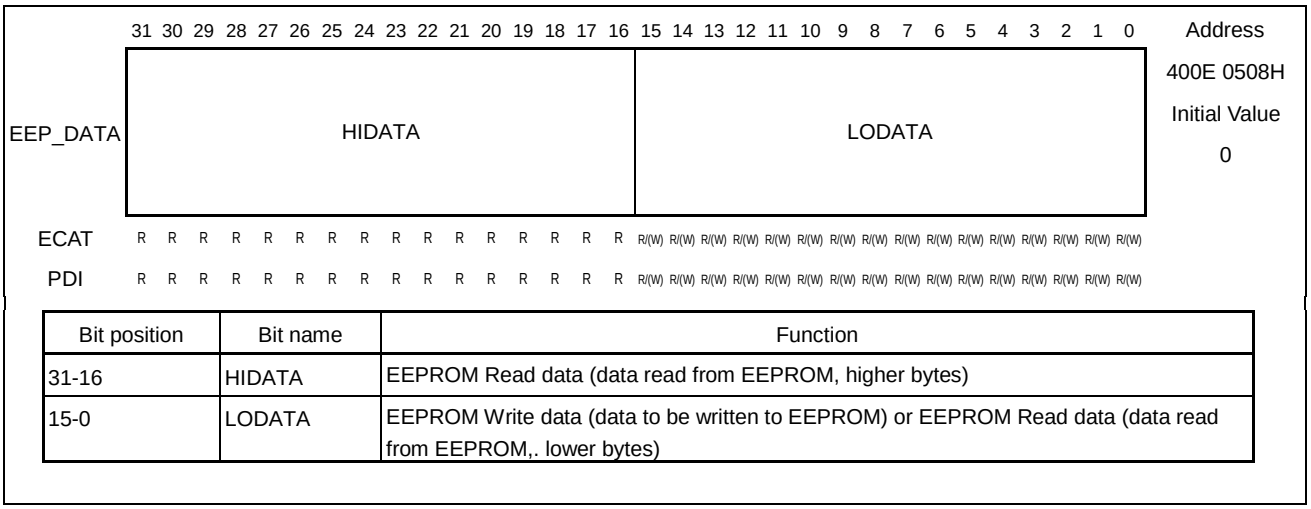


Bit position	Bit name	Function
31-0	ADDRESS	EEPROM Address 0: First word (= 16 bit) 1: Second word ... Actually used EEPROM Address bits: [9:0]: EEPROM size up to 16 kBit [17:0]: EEPROM size 32 kBit – 4 Mbit

Note Write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if EEPROM interface is busy (0x0502.15=1).

6.16.5 EEPROM Data register (EEP_DATA)

This register is used to set write data to EEPROM or indicates read data from EEPROM. It is possible to write each 1 word and read each 2 words.



Bit position	Bit name	Function
31-16	HIDATA	EEPROM Read data (data read from EEPROM, higher bytes)
15-0	LODATA	EEPROM Write data (data to be written to EEPROM) or EEPROM Read data (data read from EEPROM,. lower bytes)

Note Write access depends upon the assignment of the EEPROM interface (ECAT/PDI). Write access is generally blocked if EEPROM interface is busy (0x0502.15=1).

6.17 MII Management Interface Registers

6.17.1 MII Management Control/Status register (MII_CONT_STAT)

This register is used to control MII management interface and to indicate the status.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
MII_CONT_STAT	BUSY	CMDERR	READERR	0	0	0	COMMAND		PHYOFFSET					MILINK	PDICTRL	WREN	400E 0510H	0006H
ECAT	R	R	R/(W)	0	0	0	R/(W)	R/(W)	R	R	R	R	R	R	R	R/(W)		
PDI	R	R	R/(W)	0	0	0	R/(W)	R/(W)	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15	BUSY	Busy: 0: MI control state machine is idle 1: MI control state machine is active
14	CMDERR	Command error: 0: Last Command was successful 1: Invalid command or write command without Write Enable Cleared with a valid command or by writing "00" to Command register bits [9:8].
13	READERR	Read error: 0: No read error 1: Read error occurred (PHY or register not available) Cleared by writing to this register.
9-8	COMMAND	Command register: Write: Initiate command. Read: Currently executed command Commands: 00: No command/MI idle (clear error bits) 01: Read 10: Write Others: Reserved/invalid commands (do not issue)
7-3	PHYOFFSET	PHY address offset
2	MILINK	MI link detection (link configuration, link detection, registers 0x0518-0x051B): 0: Not available 1: MI link detection active
1	PDICTRL	Management Interface can be controlled by PDI (registers 0x0516-0 x0517): 0: Only ECAT control 1: PDI control possible
0	WREN	Write enable: 0: Write disabled 1: Write enabled This bit is always 1 if PDI has MI control.

Note Write access depends on assignment of MI (ECAT/PDI). Write access is generally blocked if Management interface is busy (0x0510.15=1).

Caution Write enable bit 0 is self-clearing at the SOF of the next frame (or at the end of the PDI access), Command bits
[9:8] are self-clearing after the command is executed (Busy ends). Writing "00" to the command register will also
clear the error bits [14:13]. The Command bits are cleared after the command is executed.

6.17.2 PHY Address register (PHY_ADR)

This register is used to set PHY address.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_ADR	0	0	0	PHYADDR					400E 0512H	00H
ECAT	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit position	Bit name	Function
4-0	PHYADDR	PHY address

Note Write access depends on assignment of MI (ECAT/PDI). Write access is generally blocked if Management interface is busy (0x0510.15=1).

6.17.3 PHY Register Address register (PHY_REG_ADR)

This register is used to set PHY register address.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_REG_ADR	0	0	0	PHYREGADDR					400E 0513H	00H
ECAT	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	0	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit position	Bit name	Function
4-0	PHYREGADDR	Address of PHY Register that shall be read/written

Note Write access depends on assignment of MI (ECAT/PDI). Write access is generally blocked if Management interface is busy (0x0510.15=1).

6.17.4 PHY Data register (PHY_DATA)

This register is used to set data to write to PHY register or to indicate read data from PHY register.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_DATA	PHYREGDATA																400E 0514H	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit position	Bit name	Function
15-0	PHYREGDATA	PHY Read/Write Data

Note Write access depends on assignment of MI (ECAT/PDI). Write access is generally blocked if Management interface is busy (0x0510.15=1).

6.17.5 MII Management ECAT Access State register (MII_ECAT_ACS_STAT)

This register is used to set access state of MII management interface.

	7	6	5	4	3	2	1	0	Address	Initial Value
MII_ECAT_ACS_STAT	0	0	0	0	0	0	0	ACSMII	400E 0516H	00H
ECAT	0	0	0	0	0	0	0	R/(W)		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	ACSMII	Access to MII management: 0: ECAT enables PDI takeover of MII management control 1: ECAT claims exclusive access to MII management

Note Write access is only possible if 0x0517.0=0.

6.17.6 MII Management PDI Access State register (MII_PDI_ACS_STAT)

This register is used to set access state of MII management interface.

	7	6	5	4	3	2	1	0	Address	Initial Value
MII_PDI_ ACS_STAT	0	0	0	0	0	0	FORPDI	ACSMII	400E 0517H	00H
ECAT	0	0	0	0	0	0	R/W	R		
PDI	0	0	0	0	0	0	R	R/(W)		

Bit position	Bit name	Function
1	FORPDI	Force PDI Access State: 0: Do not change Bit 0x0517.0 1: Reset Bit 0x0517.0 to 0
0	ACSMII	Access to MII management: 0: ECAT has access to MII management 1: PDI has access to MII management

Note Write access to bit 0 is only possible if 0x0516.0=0 and 0x0517.1=0.

6.17.7 PHY Port Status n register (PHY_STATUSn)

This register indicates PHY port status each port.

	7	6	5	4	3	2	1	0	Address	Initial Value
PHY_ STATUSn	0	0	PHYCONFIG	LINKPARTERR	READERR	LINKSTAERR	LINKSTA	PHYLINKSTA	400E 0518H + 0001H*n	00H
ECAT	0	0	R/(W/clr)	R	R/(W/clr)	R	R	R		
PDI	0	0	R/(W/clr)	R	R/(W/clr)	R	R	R		

Bit position	Bit name	Function
5	PHYCONFIG	PHY configuration updated: 0: No update 1: PHY configuration was updated Cleared by writing any value to at least one of the PHY Status Port n registers.
4	LINKPARTERR	Link partner error: 0: No error detected 1: Link partner error
3	READERR	Read error: 0: No read error occurred 1: A read error has occurred Cleared by writing any value to at least one of the PHY Status Port n registers.
2	LINKSTAERR	Link status error: 0: No error 1: Link error, link inhibited
1	LINKSTA	Link status (100 Mbit/s, Full Duplex, Autonegotiation): 0: No link 1: Link detected
0	PHYLINKSTA	Physical link status (PHY status register 1.2): 0: No physical link 1: Physical link detected

Note1 n=0-1
n=0 : Port 0, n=1 : Port 1
2 Write access depends on assignment of MI (ECAT/PDI).

6.18 FMMU Registers

6.18.1 FMMU Logical Start Address m register (FMMUm.L_START_ADR)

This register is used to set the logical start address within the EtherCAT Address Space.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
FMMUm. L_START_ ADR	LSTAADR																																400E 0600H + 0010H*m Initial Value 0000 0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

Bit position	Bit name	Function
31-0	LSTAADR	Logical start address within the EtherCAT Address Space.

Note m=0-7

6.18.2 FMMU Length m register (FMMUm.LEN)

This register is used to set the length for FMMU area.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm. LEN	FMMULEN																400E 0604H + 0010H*m	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	FMMULEN	Offset from the first logical FMMU Byte to the last FMMU Byte + 1 (e.g., if two bytes are used then this parameter shall contain 2)

Note m=0-7

6.18.3 FMMU Logical Start bit m register (FMMUm.L_START_BIT)

This register is used to set logical starting bit shall be mapped.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.L_START_BIT	0	0	0	0	0	LSTABIT			400E 0606H + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2-0	LSTABIT	Logical starting bit that shall be mapped (bits are counted from least significant bit (=0) to most significant bit(=7)

Note m=0-7

6.18.4 FMMU Logical Stop bit m register (FMMUm.L_STOP_BIT)

This register is used to set last logical bit shall be mapped.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm.L_STOP_BIT	0	0	0	0	0	LSTPBIT			400E 0607H + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2-0	LSTPBIT	Last logical bit that shall be mapped (bits are counted from least significant bit (=0) to most significant bit(=7)

Note m=0-7

6.18.5 FMMU Physical Start Address m register (FMMUm.P_START_ADR)

This register is used to set physical start address of the ESC for FMMU area.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm. P_START_ADR	PHYSTAADR																400E 0608H + 0010H*m	0000H
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	PHYSTAADR	Physical Start Address (mapped to logical Start address)

Note m=0-7

6.18.6 FMMU Physical Start bit m register (FMMUm.P_START_BIT)

This register is used to set physical starting bit of the ESC for FMMU area.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm. P_START_BIT	0	0	0	0	0	PHYSTABIT			400E 060AH + 0010H*m	00H
ECAT	0	0	0	0	0	R/W	R/W	R/W		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2-0	PHYSTABIT	Physical starting bit as target of logical start bit mapping (bits are counted from least significant bit (=0) to most significant bit(=7)

Note m=0-7

6.18.7 FMMU Type m register (FMMUm.TYPE)

This register is used to set FMMU access type.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm. TYPE	0	0	0	0	0	0	WRITE	READ	400E 060BH + 0010H*m	00H
ECAT	0	0	0	0	0	0	R/W	R/W		
PDI	0	0	0	0	0	0	R	R		

Bit position	Bit name	Function
1	WRITE	Write access mapping: 0: Ignore mapping for write accesses 1: Use mapping for write accesses
0	READ	Read access mapping: 0: Ignore mapping for read accesses 1: Use mapping for read accesses

Note m=0-7

6.18.8 FMMU Activate m register (FMMUm.ACT)

This register is used to activate FMMU.

	7	6	5	4	3	2	1	0	Address	Initial Value
FMMUm. ACT	0	0	0	0	0	0	0	ACTIVATE	400E 060CH + 0010H*m	00H
ECAT	0	0	0	0	0	0	0	R/W		
PDI	0	0	0	0	0	0	0	R		

Bit position	Bit name	Function
0	ACTIVATE	Activate FMMU: 0: FMMU deactivated 1: FMMU activated. FMMU checks logical addressed blocks to be mapped according to mapping configured.

Note m=0-7

6.19 SyncManager Registers

6.19.1 SyncManager Physical Start Address m register (SMm.P_START_ADR)

This register is used to set the physical start address for SyncManager.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. P_START_ADR	SMSTAADDR																400E 0800H + 0008H*m	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	SMSTAADDR	Specifies first byte that will be handled by SyncManager.

Note 1 m=0-7

2 Register can only be written if SyncManager is disabled (+0x6.0 = 0).

6.19.2 SyncManager Length m register (SMm.LEN)

This register is used to set the length for SyncManager area.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. LEN	SMLEN																400E 0802H + 0008H*m	0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	SMLEN	Number of bytes assigned to SyncManager (shall be greater 1, otherwise SyncManager is not activated. If set to 1, only Watchdog Trigger is generated if configured)

Note 1 m=0-7

2 Register can only be written if SyncManager is disabled (+0x6.0 = 0).

6.19.3 SyncManager Control m register (SMm.CONTROL)

This register is used to control SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. CONTROL	0	WDTRGEN	IRQPDI	IRQECAT	DIR		OPEMODE		400E 0804H + 0008H*m	00H
ECAT	0	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	0	R	R	R	R	R	R	R		

Bit position	Bit name	Function
6	WDTRGEN	Watchdog Trigger Enable: 0: Disabled 1: Enabled
5	IRQPDI	Interrupt in PDI Event Request Register: 0: Disabled 1: Enabled
4	IRQECAT	Interrupt in ECAT Event Request Register: 0: Disabled 1: Enabled
3-2	DIR	Direction: 00: Read: ECAT read access, PDI write access. 01: Write: ECAT write access, PDI read access. 10: Reserved 11: Reserved
1-0	OPEMODE	Operation Mode: 00: Buffered (3 buffer mode) 01: Reserved 10: Mailbox (Single buffer mode) 11: Reserved

Note 1 m=0-7

2 Register can only be written if SyncManager is disabled (+0x6.0 = 0).

6.19.4 SyncManager Status m register (SMm.STATUS)

This register indicates the status of SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. STATUS	WRBUF	RDBUF	BUFFERED		MAILBOX	0	INTRD	INTWR	400E 0805H + 0008H*m	30H
ECAT	R	R	R	R	R	0	R	R		
PDI	R	R	R	R	R	0	R	R		

Bit position	Bit name	Function
7	WRBUF	Write buffer in use (opened)
6	RDBUF	Read buffer in use (opened)
5-4	BUFFERED	Buffered mode: buffer status (last written buffer): 00: 1. buffer 01: 2. buffer 10: 3. buffer 11: (no buffer written) Mailbox mode: reserved
3	MAILBOX	Mailbox mode: mailbox status: 0: Mailbox empty 1: Mailbox full Buffered mode: reserved
1	INTRD	Interrupt Read: 1: Interrupt after buffer was completely and successful read 0: Interrupt cleared after first byte of buffer was written
0	INTWR	Interrupt Write: 1: Interrupt after buffer was completely and successfully written 0: Interrupt cleared after first byte of buffer was read

Note m=0-7

6.19.5 SyncManager Activate m register (SMm.ACT)

This register is used to activate SyncManager.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. ACT	LATCHPDI	LATCHECAT	0	0	0	0	REPEATREQ	SMEN	400E 0806H + 0008H*m	00H
ECAT	R/W	R/W	0	0	0	0	R/W	R/W		
PDI	R(ack)	R(ack)	0	0	0	0	R(ack)	R(ack)		

Bit position	Bit name	Function
7	LATCHPDI	Latch Event PDI: 0: No 1: Generate Latch events if PDI issues a buffer exchange or if PDI accesses buffer start address
6	LATCHECAT	Latch Event ECAT: 0: No 1: Generate Latch event if EtherCAT master issues a buffer exchange
1	REPEATREQ	Repeat Request: A toggle of Repeat Request means that a mailbox retry is needed (primarily used in conjunction with ECAT Read Mailbox)
0	SMEN	SyncManager Enable/Disable: 0: Disable: Access to Memory without SyncManager control 1: Enable: SyncManager is active and controls Memory area set in configuration

Note 1 m=0-7

2 Reading this register from PDI in all SyncManagers which have changed activation clears AL Event Request 0x0220[4]

6.19.6 SyncManager PDI Control m register (SMm.PDI_CONT)

This register is used to control SyncManager from PDI.

	7	6	5	4	3	2	1	0	Address	Initial Value
SMm. PDI_CONT	0	0	0	0	0	0	REPEATACK	DEACTIVE	400E 0807H + 0008H*m	00H
ECAT	0	0	0	0	0	0	R	R		
PDI	0	0	0	0	0	0	R/W	R/W		

Bit position	Bit name	Function
1	REPEATACK	Repeat Ack: If this is set to the same value as set by Repeat Request, the PDI acknowledges the execution of a previous set Repeat request.
0	DEACTIVE	Deactivate SyncManager: Read: 0: Normal operation, SyncManager activated. 1: SyncManager deactivated and reset SyncManager locks access to Memory area. Write: 0: Activate SyncManager 1: Request SyncManager deactivation NOTE: Writing 1 is delayed until the end of a frame which is currently processed.

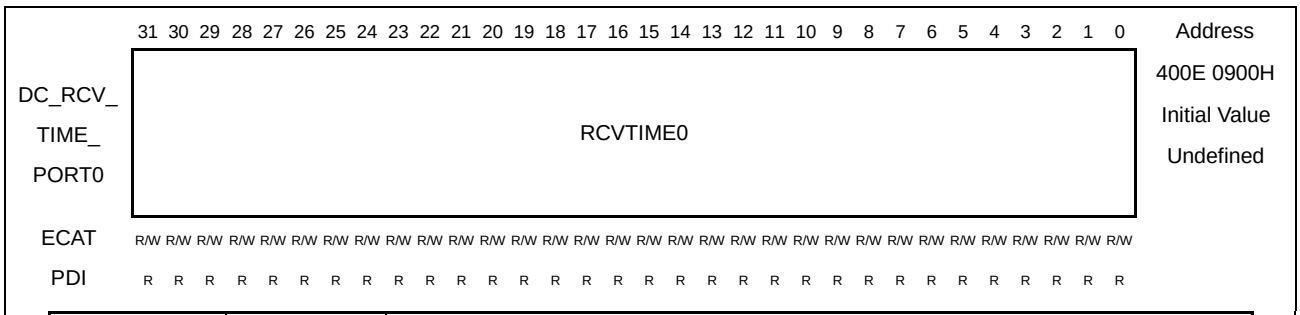
Note m=0-7

6.20 Distributed Clocks Registers

6.20.1 DC Receive Times Registers

6.20.1.1 Receive Times Port0 register (DC_RCV_TIME_PORT0)

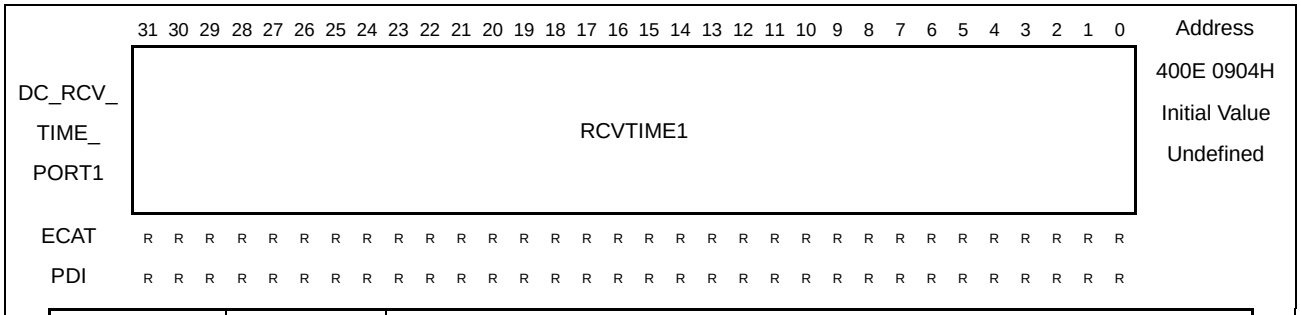
This register is used to latch receive time of the frame at all ports if write to this register and to indicate the receive time latched at port 0 if read this register.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 0900H
Initial Value
Undefined
DC_RCV_
TIME_
PORT0
RCVTIME0
ECAT
PDI
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31-0	RCVTIME0	Write: A write access to register 0x0900 with BWR, APWR (any address) or FPWR (configured address) latches the local time of the beginning of the receive frame (start first bit of preamble) at each port. Read: Local time of the beginning of the last receive frame containing a write access to this register. NOTE: The time stamps cannot be read in the same frame in which this register was written.

6.20.1.2 Receive Times Port1 register (DC_RCV_TIME_PORT1)

This register indicates received time of the frame latched at port 1.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 0904H
Initial Value
Undefined
DC_RCV_
TIME_
PORT1
RCVTIME1
ECAT
PDI
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31-0	RCVTIME1	Local time of the beginning of a frame (start first bit of preamble) received at port 1 containing a BWR/APWR or FPWR to Register 0x0900.

6.20.2 DC Time Loop Control Unit Registers

6.20.2.1 System Time register (DC_SYS_TIME)

This register indicates local copy of the System Time.

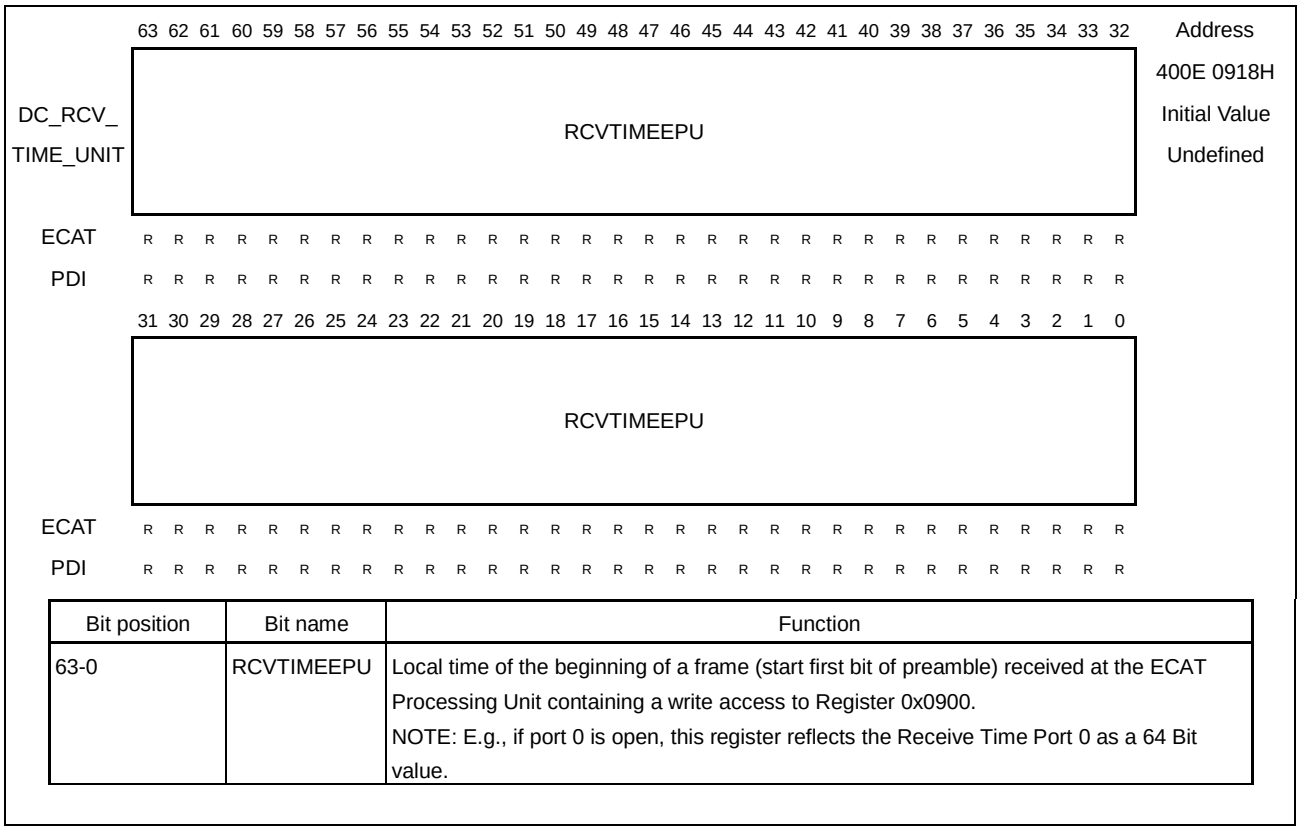
	63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	Address
DC_SYS_TIME	SYSTIME																																400E 0910H Initial Value 0000 0000 0000 0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SYSTIME																															
ECAT	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit position	Bit name	Function
63-0	SYSTIME	Access from ECAT Read: Local copy of the System Time when the frame passed the reference clock (i.e., including System Time Delay). Time latched at beginning of the frame (Ethernet SOF delimiter) Write: Written value will be compared with the local copy of the System time. The result is an input to the time control loop. NOTE: written value will be compared at the end of the frame with the latched (SOF) local copy of the System time if at least the first byte (0x0910) was written.
		Access from PDI Read: Local copy of the System Time. Time latched when reading first byte (0x0910)

6.20.2.2 Receive Time ECAT Processing Unit register (DC_RCV_TIME_UNIT)

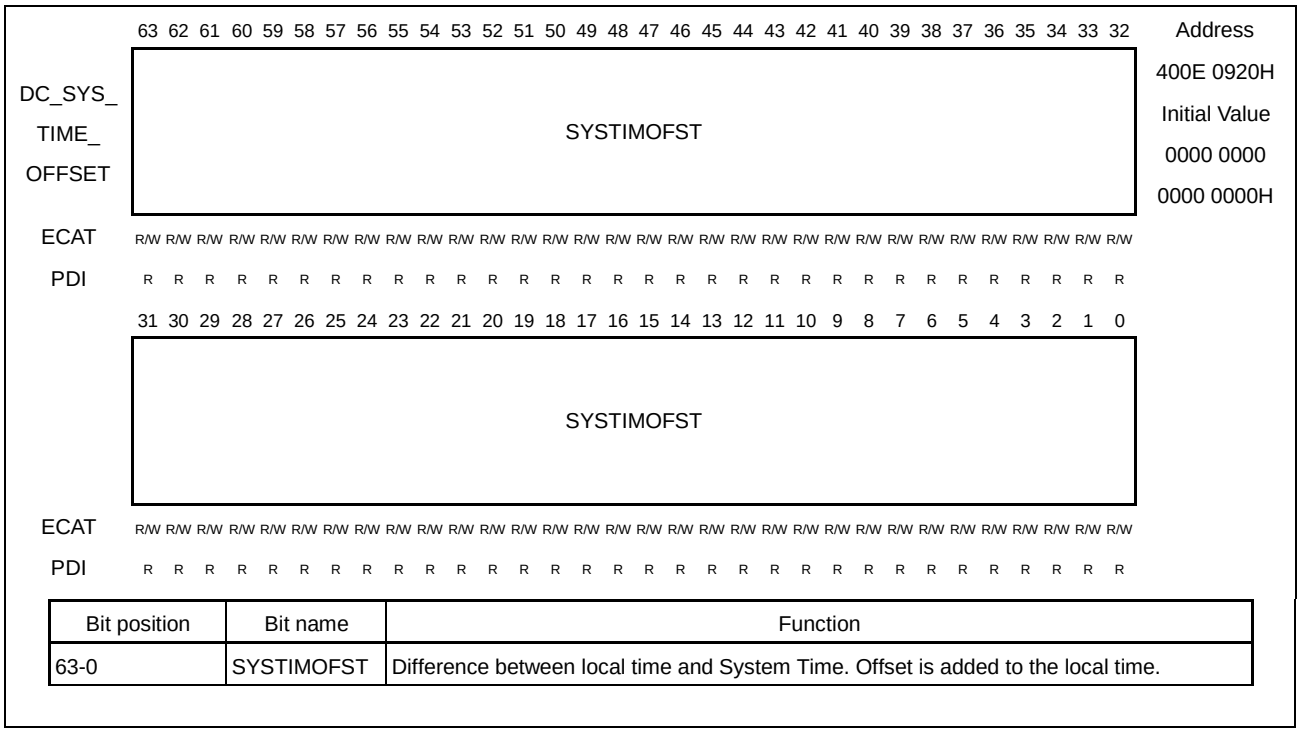
This register indicates received time of the frame latched at EtherCAT Processing Unit.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 0918H
Initial Value
Undefined
DC_RCV_
TIME_UNIT
RCVTIMEEPU
ECAT
PDI
R R R R R R R R R R R R R R R R R R R R R R R R R R R R
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
RCVTIMEEPU
ECAT
PDI
R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
63-0	RCVTIMEEPU	Local time of the beginning of a frame (start first bit of preamble) received at the ECAT Processing Unit containing a write access to Register 0x0900. NOTE: E.g., if port 0 is open, this register reflects the Receive Time Port 0 as a 64 Bit value.

6.20.2.3 System Time Offset register (DC_SYS_TIME_OFFSET)

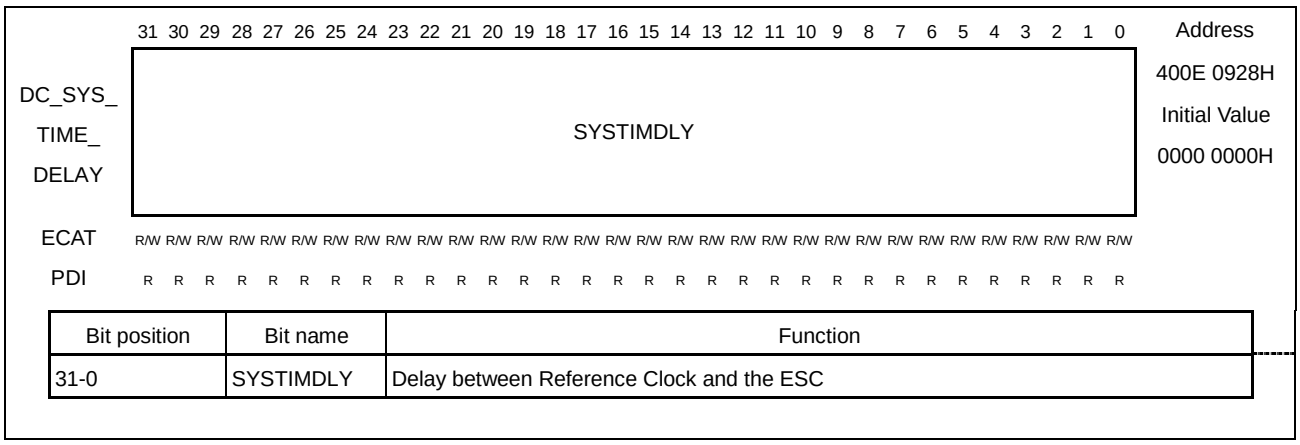
This register is used to indicate difference between local time and System Time.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 0920H
Initial Value
0000 0000
0000 0000H
DC_SYS_
TIME_
OFFSET
SYSTIMOFST
ECAT
PDI
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SYSTIMOFST
ECAT
PDI
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
63-0	SYSTIMOFST	Difference between local time and System Time. Offset is added to the local time.

6.20.2.4 System Time Delay register (DC_SYS_TIME_DELAY)

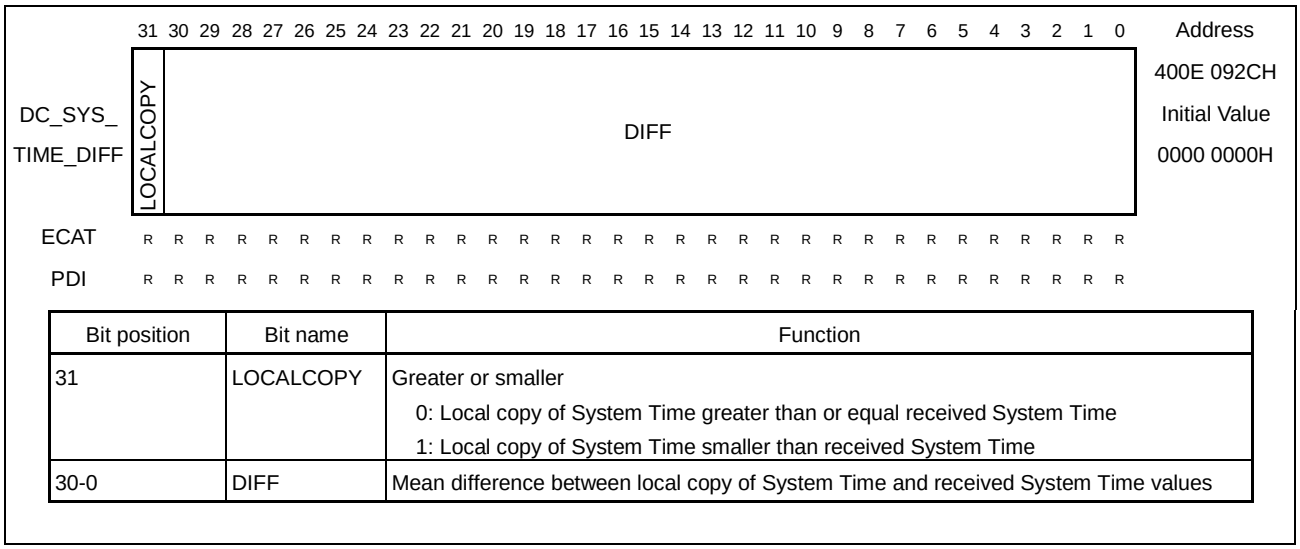
This register indicates propagation delay between Reference Clock and the ESC.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 0928H
Initial Value
0000 0000H
DC_SYS_
TIME_
DELAY
SYSTIMDLY
ECAT
PDI
R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31-0	SYSTIMDLY	Delay between Reference Clock and the ESC

6.20.2.5 System Time Difference register (DC_SYS_TIME_DIFF)

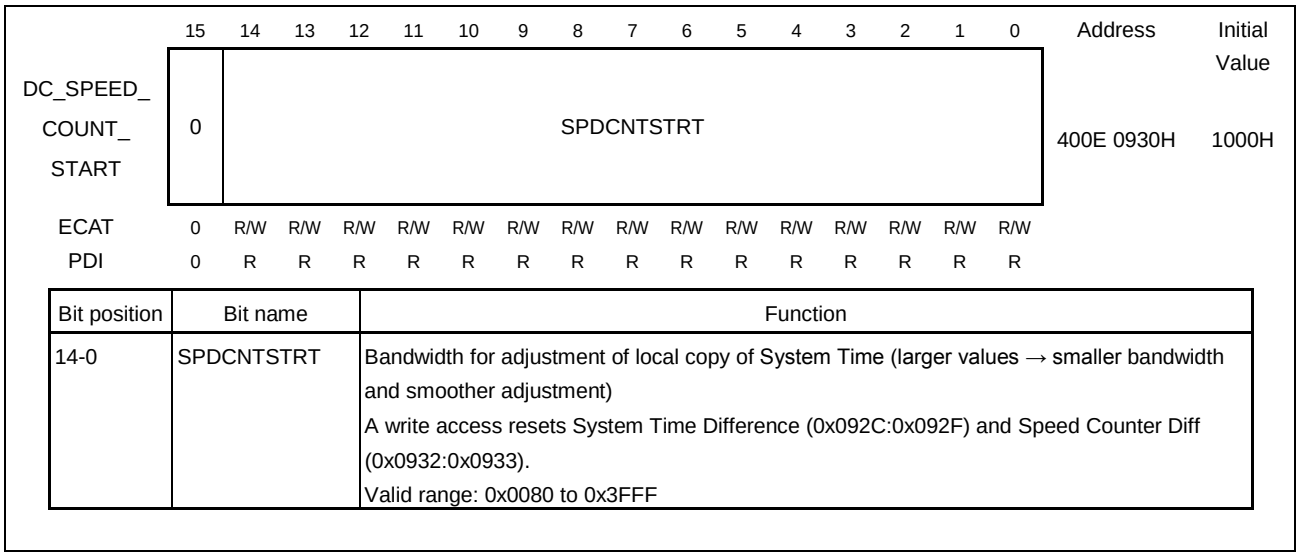
This register indicates mean difference between local copy of System Time and received System Time.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 092CH
Initial Value
0000 0000H
DC_SYS_TIME_DIFF
LOCALCOPY
DIFF
ECAT R R R R R R R R R R R R R R R R R R R R R R R R R R R R
PDI R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31	LOCALCOPY	Greater or smaller 0: Local copy of System Time greater than or equal received System Time 1: Local copy of System Time smaller than received System Time
30-0	DIFF	Mean difference between local copy of System Time and received System Time values

6.20.2.6 Speed Counter Start register (DC_SPEED_COUNT_START)

This register is used to set bandwidth for adjustment of local copy of System Time.


15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
Initial Value
DC_SPEED_COUNT_START
0
SPDCNTSTRT
400E 0930H
1000H
ECAT 0 R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W R/W
PDI 0 R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
14-0	SPDCNTSTRT	Bandwidth for adjustment of local copy of System Time (larger values → smaller bandwidth and smoother adjustment) A write access resets System Time Difference (0x092C:0x092F) and Speed Counter Diff (0x0932:0x0933). Valid range: 0x0080 to 0x3FFF

6.20.2.7 Speed Counter Diff register (DC_SPEED_COUNT_DIFF)

This register indicates the deviation between local clock period and Reference Clock's clock period.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SPEED_COUNT_DIFF	SPDCNTDIFF																400E 0932H	0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	SPDCNTDIFF	Representation of the deviation between local clock period and Reference Clock's clock period (representation: two's complement) Range: ±(Speed Counter Start – 0x7F)

6.20.2.8 System Time Difference Filter Depth register (DC_SYS_TIME_DIFF_FIL_DEPTH)

This register is used to set filter depth for averaging the received System Time deviation.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYS_TIME_DIFF_FIL_DEPTH	0	0	0	0	SYSTIMDEP				400E 0934H	04H
ECAT	0	0	0	0	R/W	R/W	R/W	R/W		
PDI	0	0	0	0	R	R	R	R		

Bit position	Bit name	Function
3-0	SYSTIMDEP	Filter depth for averaging the received System Time deviation A write access resets System Time Difference (0x092C:0x092F)

6.20.2.9 Speed Counter Filter Depth register (DC_SPEED_COUNT_FIL_DEPTH)

This register is used to set filter depth for averaging the clock period deviation.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SPEED_COUNT_FIL_DEPTH	0	0	0	0	CLKPERDEP				400E 0935H	0CH
ECAT	0	0	0	0	R/W	R/W	R/W	R/W		
PDI	0	0	0	0	R	R	R	R		

Bit position	Bit name	Function
3-0	CLKPERDEP	Filter depth for averaging the clock period deviation A write access resets the internal speed counter filter.

6.20.3 Cyclic Unit Control Registers

6.20.3.1 Cyclic Unit Control register (DC_CYC_CONT)

This register is used to control cyclic unit.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_CYC_CONT	0	0	LATCH1	LATCH0	0	0	0	SYNCOUT	400E 0980H	00H
ECAT	0	0	R/W	R/W	0	0	0	R/W		
PDI	0	0	R	R	0	0	0	R		

Bit position	Bit name	Function
5	LATCH1	Latch In unit 1: 0: ECAT controlled 1: PDI controlled NOTE: Latch interrupt is routed to ECAT/PDI depending on this setting
4	LATCH0	Latch In unit 0: 0: ECAT controlled 1: PDI controlled NOTE: Always 1 (PDI controlled) if System Time is PDI controlled. Latch interrupt is routed to ECAT/PDI depending on this setting
0	SYNCOUT	SYNC out unit control: 0: ECAT controlled 1: PDI controlled

6.20.4 SYNC Out Unit Registers

6.20.4.1 Activation register (DC_ACT)

This register is used to activate Sync Out Unit.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_ACT	DBGPULSE	NEARFUTURE	STARTTIME	EXTSTARTTIME	AUTOACT	SYNC1	SYNC0	SYNCACT	400E 0981H	00H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)		

Bit position	Bit name	Function
7	DBGPULSE	SyncSignal debug pulse (Vasili bit): 0: Deactivated 1: Immediately generate a single debug ping on SYNC0 and SYNC1 according to 0x0981[2:1] This bit is self-clearing, always read 0.
6	NEARFUTURE	Near future configuration (approx.): 0: ½ DC width future (2^{31} ns or 2^{63} ns) 1: 2.1 sec. future (2^{31} ns)
5	STARTTIME	Start Time plausibility check: 0: Disabled. SyncSignal generation if Start Time is reached. 1: Immediate SyncSignal generation if Start Time is outside near future (see 0x0981.6)
4	EXTSTARTTIME	Extension of Start Time Cyclic Operation (0x0990:0x0993): 0: No extension 1: Extend 32 bit written Start Time to 64 bit
3	AUTOACT	Auto-activation by writing Start Time Cyclic Operation (0x0990:0x0997): 0: Disabled 1: Auto-activation enabled. 0x0981.0 is set automatically after Start Time is written.
2	SYNC1	SYNC1 generation: 0: Deactivated 1: SYNC1 pulse is generated
1	SYNC0	SYNC0 generation: 0: Deactivated 1: SYNC0 pulse is generated
0	SYNCACT	Sync Out Unit activation: 0: Deactivated 1: Activated NOTE: Write 1 after Start Time was written.

Note Write to this register depends upon setting of 0x0980.0.

6.20.4.2 Pulse Length of SyncSignals register (DC_PULSE_LEN)

This register indicates pulse length of SyncSignals.

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address	Initial Value
DC_PULSE_LEN	PULSELEN																400E 0982H	2710H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R		

Bit position	Bit name	Function
15-0	PULSELEN	Pulse length of SyncSignals (in Units of 10ns) 0: Acknowledge mode: SyncSignal will be cleared by reading SYNC0/SYNC1 Status register

6.20.4.3 Activation Status register (DC_ACT_STAT)

This register indicates activation status of SyncSignals.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_ACT_STAT	0	0	0	0	0	STARTTIME	SYNC1ACT	SYNC0ACT	400E 0984H	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2	STARTTIME	Start Time Cyclic Operation (0x0990:0x0997) plausibility check result when Sync Out Unit was activated: 0: Start Time was within near future 1: Start Time was out of near future (0x0981.6)
1	SYNC1ACT	SYNC1 activation state: 0: First SYNC1 pulse is not pending 1: First SYNC1 pulse is pending
0	SYNC0ACT	SYNC0 activation state: 0: First SYNC0 pulse is not pending 1: First SYNC0 pulse is pending

6.20.4.4 SYNC0 Status register (DC_SYNC0_STAT)

This register indicates SYNC0 status. It is only used in Acknowledge mode.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYNC0_STAT	0	0	0	0	0	0	0	SYNC0STA	400E 098EH	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R(ack)		

Bit position	Bit name	Function
0	SYNC0STA	SYNC0 state for Acknowledge mode. SYNC0 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode

6.20.4.5 SYNC1 Status register (DC_SYNC1_STAT)

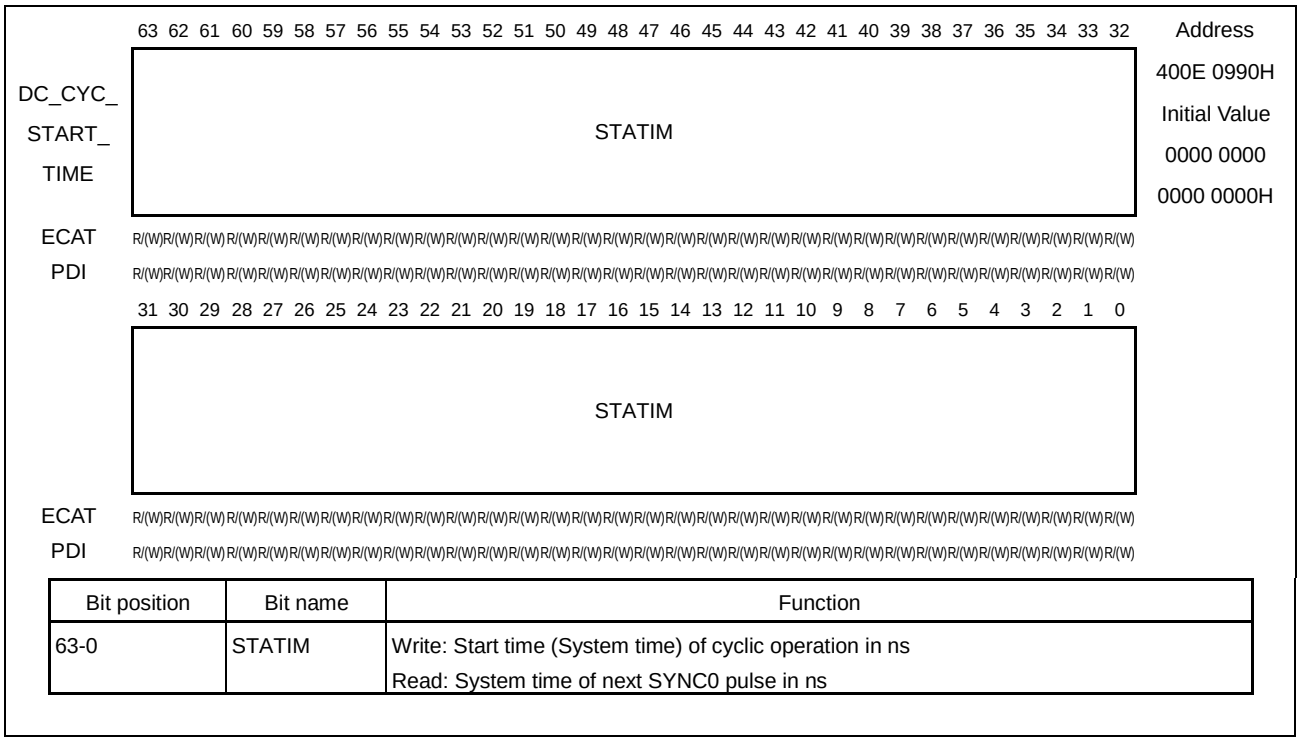
This register indicates SYNC1 status. It is only used in Acknowledge mode.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_SYNC1_STAT	0	0	0	0	0	0	0	SYNC1STA	400E 098FH	00H
ECAT	0	0	0	0	0	0	0	R		
PDI	0	0	0	0	0	0	0	R(ack)		

Bit position	Bit name	Function
0	SYNC1STA	SYNC1 state for Acknowledge mode. SYNC1 in Acknowledge mode is cleared by reading this register from PDI, use only in Acknowledge mode

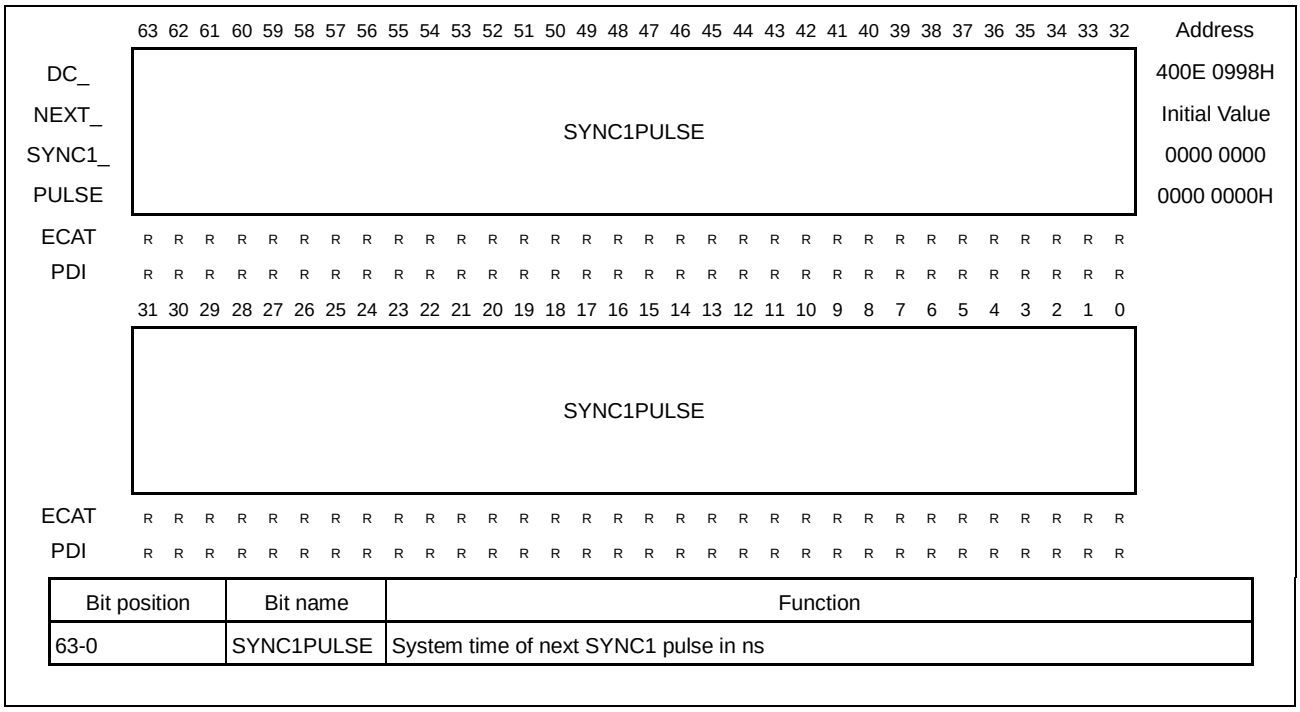
6.20.4.6 Start Time Cyclic Operation/Next SYNC0 Pulse register (DC_CYC_START_TIME)

This register is used set start time of cyclic operation if write to this register and to indicate System Time of next SYNC0 pulse if read this register.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 0990H
Initial Value
0000 0000
0000 0000H
DC_CYC_
START_
TIME
STATIM
ECAT
PDI
R/(W)R/(W)R/(W)

6.20.4.7 Next SYNC1 Pulse register (DC_NEXT_SYNC1_PULSE)

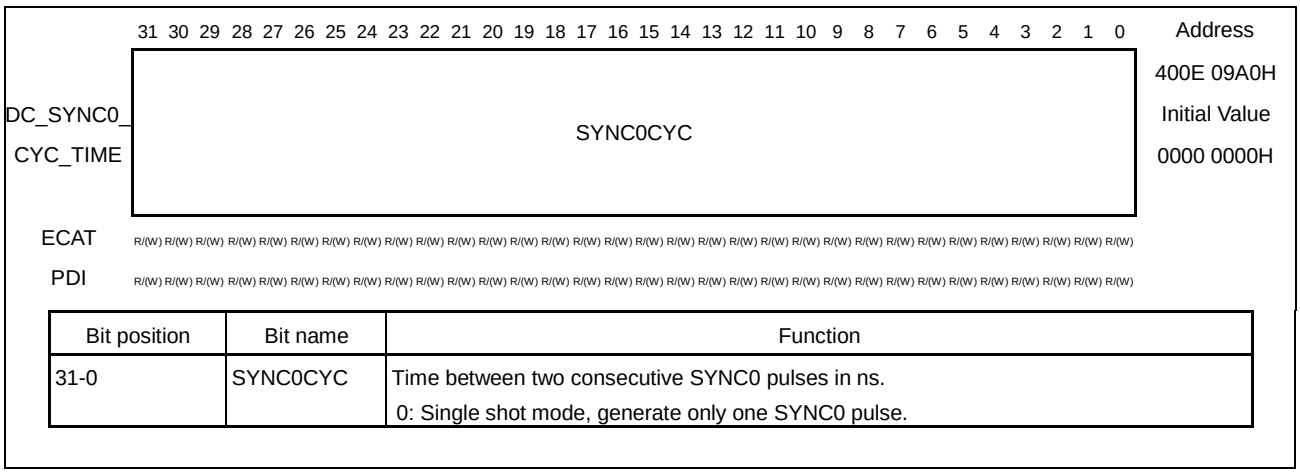
This register indicates System Time of next SYNC1 pulse.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
DC_
NEXT_
SYNC1_
PULSE
SYNC1PULSE
400E 0998H
Initial Value
0000 0000
0000 0000H
ECAT
PDI
R R R R R R R R R R R R R R R R R R R R R R R R R R R R
R R R R R R R R R R R R R R R R R R R R R R R R R R R R
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SYNC1PULSE
ECAT
PDI
R R R R R R R R R R R R R R R R R R R R R R R R R R R R
R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
63-0	SYNC1PULSE	System time of next SYNC1 pulse in ns

6.20.4.8 SYNC0 Cycle Time register (DC_SYNC0_CYC_TIME)

This register is used to set cycle time of SYNC0 pulse.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
DC_SYNC0_
CYC_TIME
SYNC0CYC
400E 09A0H
Initial Value
0000 0000H
ECAT
PDI
R/(W) R/(W)
R/(W) R/(W)

Bit position	Bit name	Function
31-0	SYNC0CYC	Time between two consecutive SYNC0 pulses in ns. 0: Single shot mode, generate only one SYNC0 pulse.

Note Write to this register depends upon setting of 0x0980.0.

6.20.4.9 SYNC1 Cycle Time register (DC_SYNC1_CYC_TIME)

This register is used to set time between SYNC1 pulse and SYNC0 pulse.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DC_SYNC1_CYC_TIME	SYNC1CYC																																400E 09A4H Initial Value 0000 0000H
ECAT	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	
PDI	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	R/(W)	

Bit position	Bit name	Function
31-0	SYNC1CYC	Time between SYNC1 pulses and SYNC0 pulse in ns

Note Write to this register depends upon setting of 0x0980.0.

6.20.5 Latch In Unit Registers

6.20.5.1 Latch0 Control register (DC_LATCH0_CONT)

This register is used to control the edge function of Latch0 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH0_CONT	0	0	0	0	0	0	NEGEDGE	POSEDGE	400E 09A8H	00H
ECAT	0	0	0	0	0	0	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	R/(W)	R/(W)		

Bit position	Bit name	Function
1	NEGEDGE	Latch0 negative edge: 0: Continuous Latch active 1: Single event (only first event active)
0	POSEDGE	Latch0 positive edge: 0: Continuous Latch active 1: Single event (only first event active)

Note Write to this register depends upon setting of 0x0980.4.

6.20.5.2 Latch1 Control register (DC_LATCH1_CONT)

This register is used to control the edge function of Latch1 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH1_CONT	0	0	0	0	0	0	NEGEDGE	POSEDGE	400E 09A9H	00H
ECAT	0	0	0	0	0	0	R/(W)	R/(W)		
PDI	0	0	0	0	0	0	R/(W)	R/(W)		

Bit position	Bit name	Function
1	NEGEDGE	Latch1 negative edge: 0: Continuous Latch active 1: Single event (only first event active)
0	POSEDGE	Latch1 positive edge: 0: Continuous Latch active 1: Single event (only first event active)

Note Write to this register depends upon setting of 0x0980.5.

6.20.5.3 Latch0 Status register (DC_LATCH0_STAT)

This register indicates the state of Latch0 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH0_STAT	0	0	0	0	0	PINSTATE	EVENTNEG	EVENTPOS	400E 09AEH	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2	PINSTATE	Latch0 pin state
1	EVENTNEG	Event Latch0 negative edge. 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only. Flag cleared by reading out Latch0 Time Negative Edge.
0	EVENTPOS	Event Latch0 positive edge. 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only. Flag cleared by reading out Latch0 Time Positive Edge.

6.20.5.4 Latch1 Status register (DC_LATCH1_STAT)

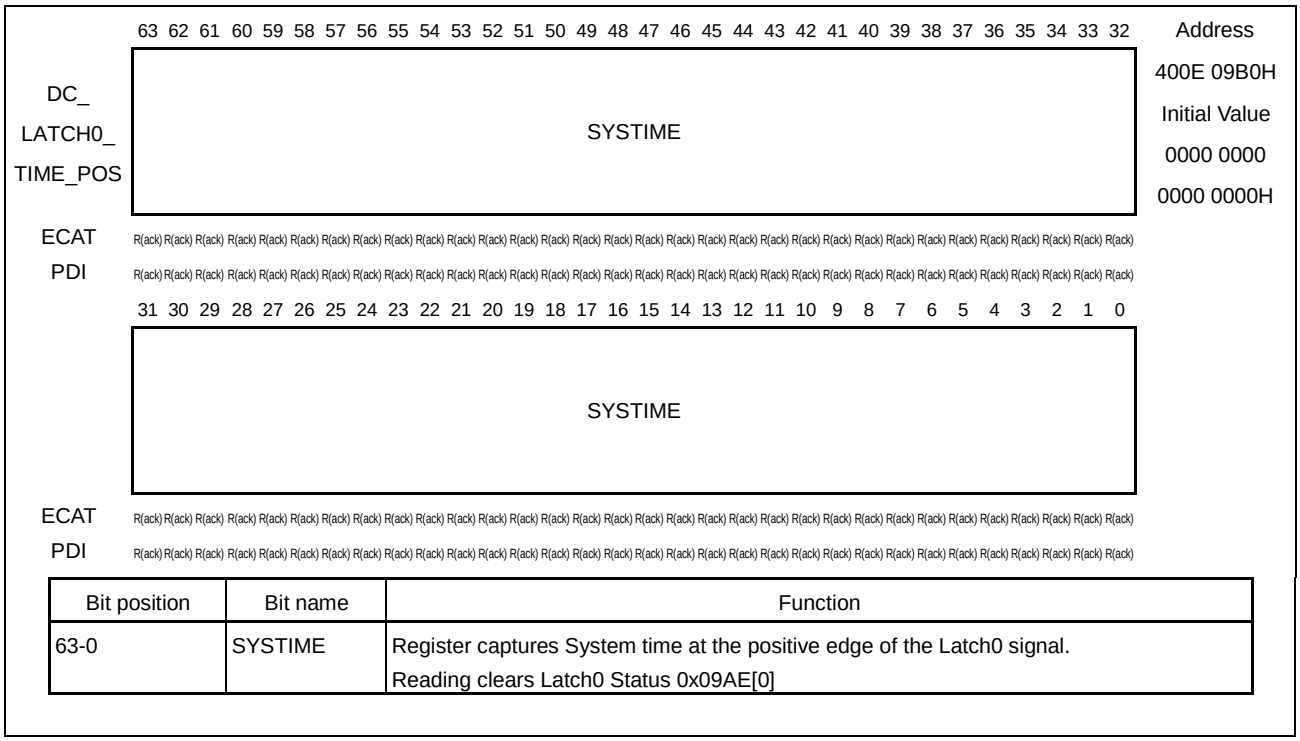
This register indicates the state of Latch1 input signal.

	7	6	5	4	3	2	1	0	Address	Initial Value
DC_LATCH1_STAT	0	0	0	0	0	PINSTATE	EVENTNEG	EVENTPOS	400E 09AFH	00H
ECAT	0	0	0	0	0	R	R	R		
PDI	0	0	0	0	0	R	R	R		

Bit position	Bit name	Function
2	PINSTATE	Latch1 pin state
1	EVENTNEG	Event Latch1 negative edge. 0: Negative edge not detected or continuous mode 1: Negative edge detected in single event mode only. Flag cleared by reading out Latch1 Time Negative Edge.
0	EVENTPOS	Event Latch1 positive edge. 0: Positive edge not detected or continuous mode 1: Positive edge detected in single event mode only. Flag cleared by reading out Latch1 Time Positive Edge.

6.20.5.5 Latch0 Time Positive Edge register (DC_LATCH0_TIME_POS)

This register indicates System time at the positive edge of the Latch0 signal.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 09B0H
Initial Value
0000 0000
0000 0000H
DC_
LATCH0_
TIME_POS
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)

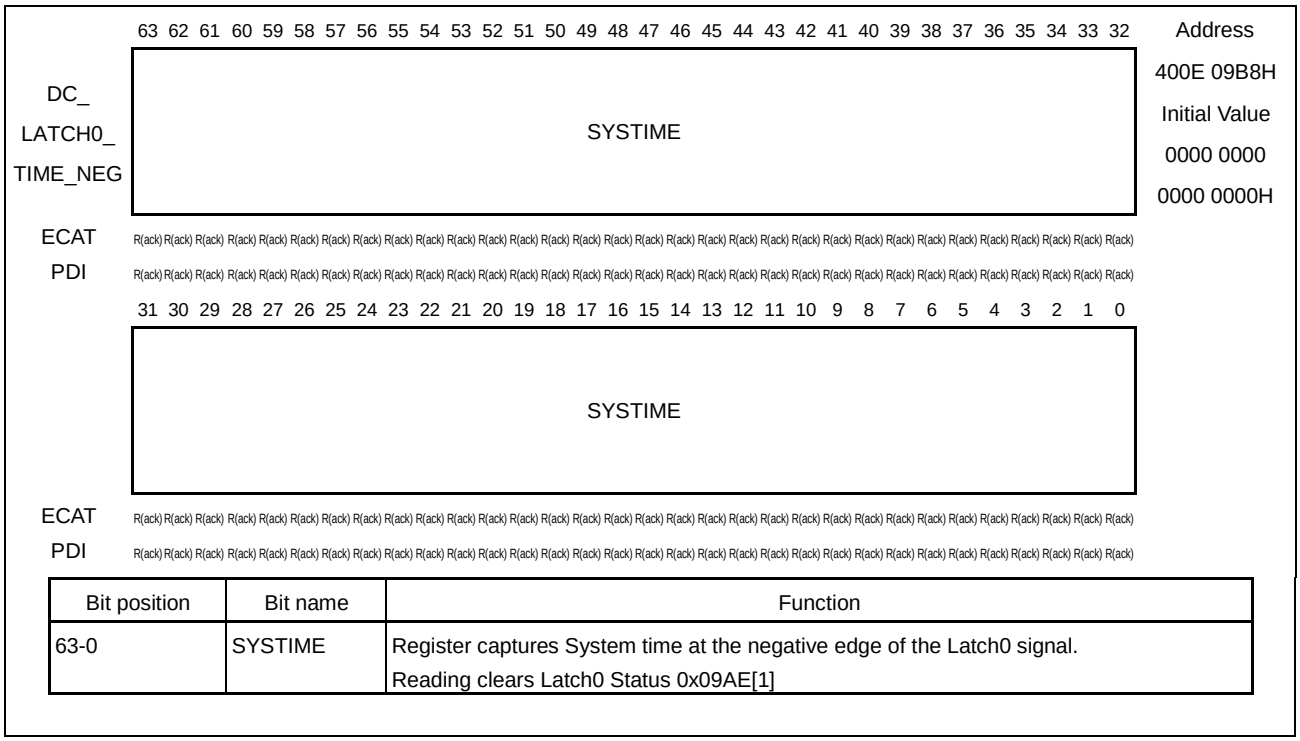
Bit position	Bit name	Function
63-0	SYSTIME	Register captures System time at the positive edge of the Latch0 signal. Reading clears Latch0 Status 0x09AE[0]

Note 1 Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

2 Clearing Latch0 Status flag function depends upon setting of 0x0980.4.

6.20.5.6 Latch0 Time Negative Edge register (DC_LATCH0_TIME_NEG)

This register indicates System time at the negative edge of the Latch0 signal.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 09B8H
Initial Value
0000 0000
0000 0000H
DC_
LATCH0_
TIME_NEG
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)

Bit position	Bit name	Function
63-0	SYSTIME	Register captures System time at the negative edge of the Latch0 signal. Reading clears Latch0 Status 0x09AE[1]

Note 1 Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

2 Clearing Latch0 Status flag function depends upon setting of 0x0980.4.

6.20.5.7 Latch1 Time Positive Edge register (DC_LATCH1_TIME_POS)

This register indicates System time at the positive edge of the Latch1 signal.

	63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32	Address
DC_LATCH1_TIME_POS	SYSTIME	400E 09C0H Initial Value 0000 0000 0000 0000H
ECAT PDI	R(ack) R(ack)	
	31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0	
	SYSTIME	
ECAT PDI	R(ack) R(ack)	

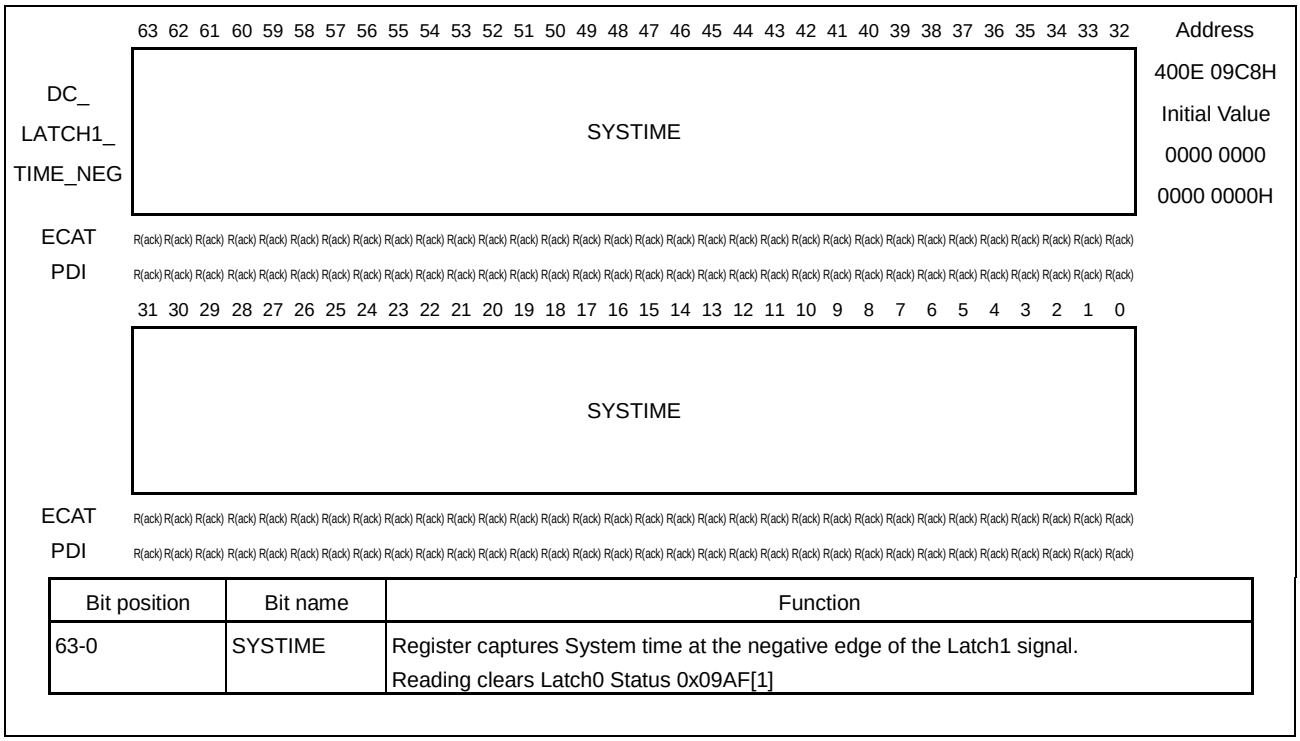
Bit position	Bit name	Function
63-0	SYSTIME	Register captures System time at the positive edge of the Latch1 signal. Reading clears Latch1 Status 0x09AF[0]

Note 1 Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

2 Clearing Latch1 Status flag function depends upon setting of 0x0980.5.

6.20.5.8 Latch1 Time Negative Edge register (DC_LATCH1_TIME_NEG)

This register indicates System time at the negative edge of the Latch1 signal.


63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32
Address
400E 09C8H
Initial Value
0000 0000
0000 0000H
DC_
LATCH1_
TIME_NEG
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
SYSTIME
ECAT
PDI
R(ack) R(ack)
R(ack) R(ack)

Bit position	Bit name	Function
63-0	SYSTIME	Register captures System time at the negative edge of the Latch1 signal. Reading clears Latch0 Status 0x09AF[1]

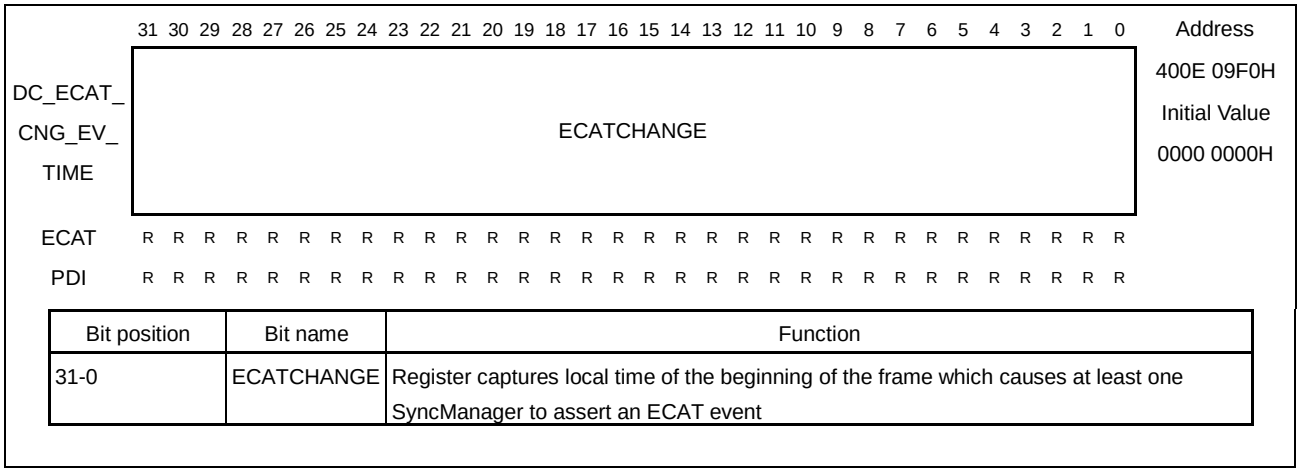
Note 1 Register bits [63:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

2 Clearing Latch1 Status flag function depends upon setting of 0x0980.5.

6.20.6 SyncManager Event Times Registers

6.20.6.1 Buffer Change Event Time register (DC_ECAT_CNG_EV_TIME)

This register indicates local time of the beginning of the frame which causes at least one SyncManager to assert an ECAT event.

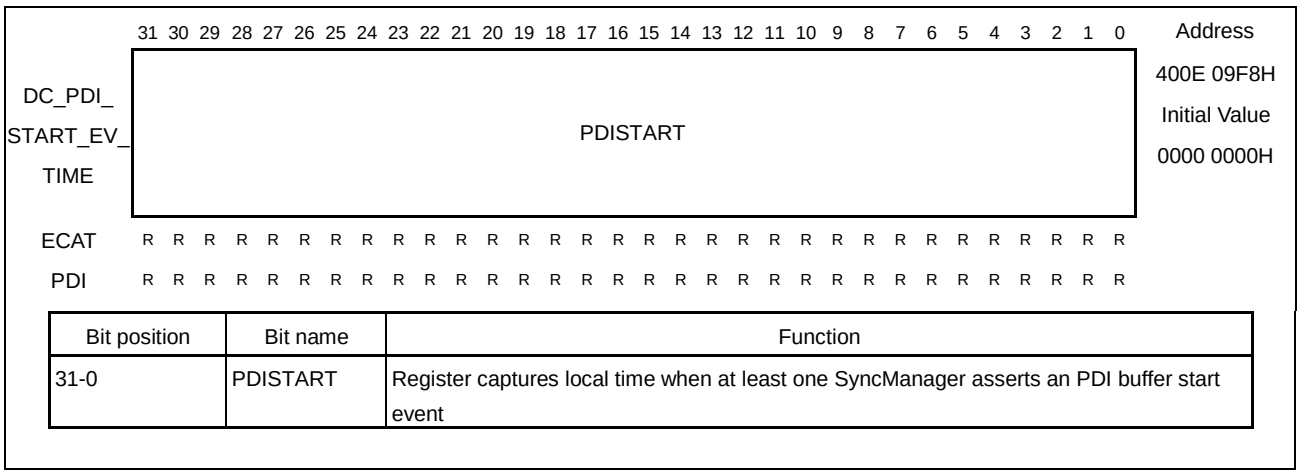

31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 09F0H
Initial Value
0000 0000H
DC_ECAT_CNG_EV_TIME
ECATCHANGE
ECAT R R R R R R R R R R R R R R R R R R R R R R R R R R R R
PDI R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31-0	ECATCHANGE	Register captures local time of the beginning of the frame which causes at least one SyncManager to assert an ECAT event

Note Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

6.20.6.2 PDI Buffer Start Event Time register (DC_PDI_START_EV_TIME)

This register indicates local time when at least one SyncManager asserts a PDI buffer start event.


31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
Address
400E 09F8H
Initial Value
0000 0000H
DC_PDI_START_EV_TIME
PDISTART
ECAT R R R R R R R R R R R R R R R R R R R R R R R R R R R R
PDI R R R R R R R R R R R R R R R R R R R R R R R R R R R R

Bit position	Bit name	Function
31-0	PDISTART	Register captures local time when at least one SyncManager asserts an PDI buffer start event

Note Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

6.20.6.3 PDI Buffer Change Event Time register (DC_PDI_CNG_EV_TIME)

This register indicates local time when at least one SyncManager asserts a PDI buffer change event.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DC_PDI_CNG_EV_TIME	PDICHANGE																																400E 09FCH Initial Value 0000 0000H
ECAT	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	
PDI	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	

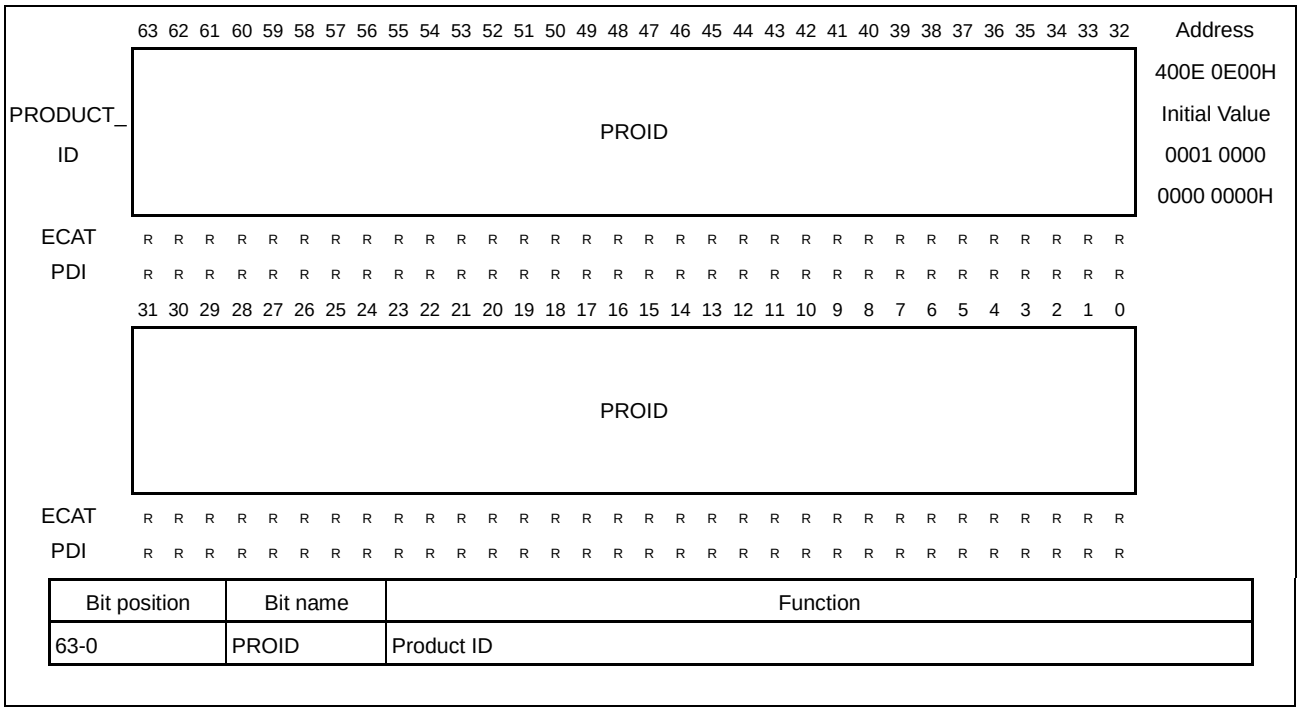
Bit position	Bit name	Function
31-0	PDICHANGE	Register captures local time when at least one SyncManager asserts an PDI buffer change event

Note Register bits [31:8] are internally latched (ECAT/PDI independently) when bits [7:0] are read, which guarantees reading a consistent value.

6.21 ETC Registers

6.21.1 PRODUCT ID register (PRODUCT_ID)

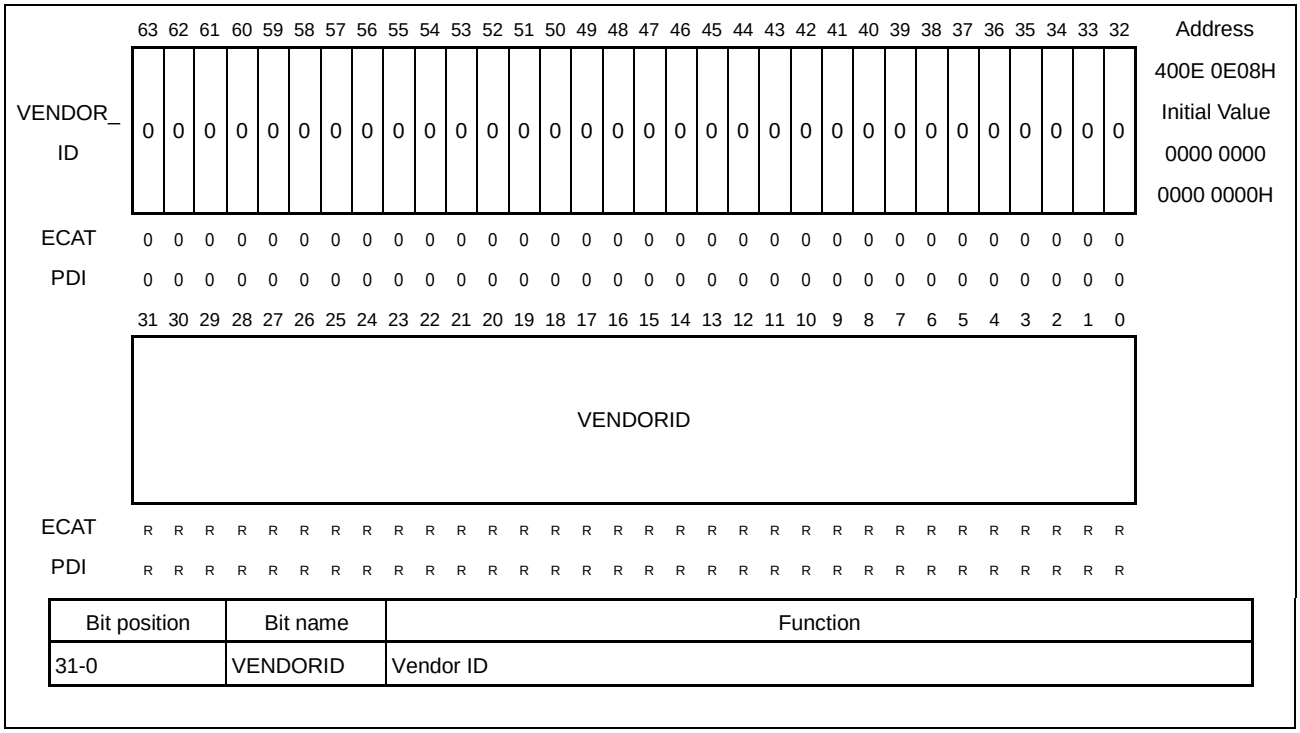
This register indicates product ID.



Bit position	Bit name	Function
63-0	PROID	Product ID

6.21.2 Vender ID register (VENDOR_ID)

This register indicates vendor ID.



Bit position	Bit name	Function
31-0	VENDORID	Vendor ID

6.21.3 User RAM (USER_RAM)

This register indicates the supported features dependent on IP core configuration. The area is 128Byte from 400E 0F80H to 400E 0FFFH. Value 1 of reset value means supported features. But bit 7-0 indicate the number of bits defined in the User RAM. The value of R-IN32M3-EC is 33H.

Bit position	Description	Reset value
7-0	Number of extended feature bits. This LSI indicates 51bits (33H).	33H
8	Extended DL Control Register (0x0102:0x0103)	1
9	AL Status Code Register (0x0134:0x0135)	1
10	ECAT Event Mask (0x0200:0x0201)	1
11	Configured Station Alias (0x0012:0x0013)	1
12	General Purpose Inputs (0x0F18:0x0F1F)	0
13	General Purpose Outputs (0x0F10:0x0F17)	0
14	AL Event Mask (0x0204:0x0207)	1
15	Physical Read/Write Offset (0x0108:0x0109)	1
16	Watchdog divider writeable (0x0400:0x04001) and Watchdog PDI (0x0410:0x0f11)	1
17	Watchdog counters (0x0442:0x0443)	1
18	Write Protection (0x0020:0x0031)	1
19	Reset (0x0040:0x0041)	1
20	Reserved	0
21	DC SyncManager Event Times (0x09F0:0x09FF)	1
22	ECAT Processing Unit/PDI Error Counter (0x030C:0x030D)	1
23	EEPROM Size configurable (0x0502.7): 0: EEPROM Size fixed to sizes up to 16 Kbit 1: EEPROM Size configurable	1
26-24	Reserved	0
27	Lost Link Counter (0x0310:0x0313)	1
28	MII Management Interface (0x0510:0x0515)	1
29	Enhanced Link Detection MII	1
30	Enhanced Link Detection EBUS	0
31	Run LED (DEV_STATE LED)	1
32	Link/Activity LED	1
33	Reserved	0
35-34	Reserved	1
36	Reserved	0
37	Reserved	1
38	DC Time loop control assigned to PDI	0
39	Link detection and configuration by MI	1
40	MI control by PDI possible	1
41	Automatic TX shift	1
42	EEPROM emulation by µController	0
49-43	Reserved	0
50	ERR LED, RUN/ERR LED Override	1
others	Reserved	Reserved

6.21.4 Process Data RAM (DATA_RAM)

This RAM is used in process data and mailbox. The area is 8Kbyte from 400E 1000H to 400E 2FFFH. Process Data Process Data RAM is only accessible if EEPROM was correctly loaded (register 0x0110.0=1).

7. Etherne PHY Function

7.1 Features

R-IN32M3-EC supports 10BASE-T, 100BASE-TX/FX and integrated IEEE802.3 dual-port Ethernet physical layer (PHY). It is possible to connect twisted-pair (UTP) cable by external pulse transformer or connect optical fiber by optical transceiver. And it supports Daisy chain structure and ring structure used by industry network.

- 10BASE-T, 100BASE-TX and 100BASE-FX of based upon IEEE802.3
- 2 port
- Auto-negotiation
- Full-duplex transmission and a half-duplex transmission
- Automatic MDI/MDI-X
- Serial management interface (MDC/MDIO)
- Low latency function
- Quick auto-negotiation
- Cable diagnosis function
- Fast link-loss Detection function (BER Monitor, FEQ Monitor)

Caution. EtherCAT Slave Controller When using EtherCAT Slave Controller, it doesn't correspond to 100BASE-FX. Please use 100BASE-TX.

7.2 Special functions

7.2.1 Low latency function

It is possible to shorten the latency time for Ethernet frame passing through PHY from LINE interface to MII interface (Low latency mode). Ethernet frame starts from preamble while this preamble starts from symbol 11000 (J) and 10001 (K) of symbol (5B) of LINE. In the devices generally based on Ethernet, it's recognized as start preamble by detecting symbol J and K. In latency function mode, it's recognized as start preamble by detecting symbol J only. This means RX_DV signal is asserted at this moment and it becomes possible to shorten the latency 40ns. If symbol J is incorrectly detected by a bit error, RX_ER signal is asserted and the receiver will continue when symbol K in the following is not received.

Low latency mode becomes effective by setting bit 1(RX_DV_J2T bit) of register 31 by 1.

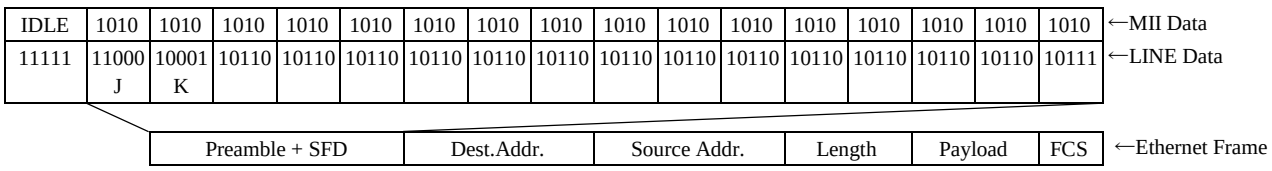


Figure 7.1 Preamble of Ethernet frames

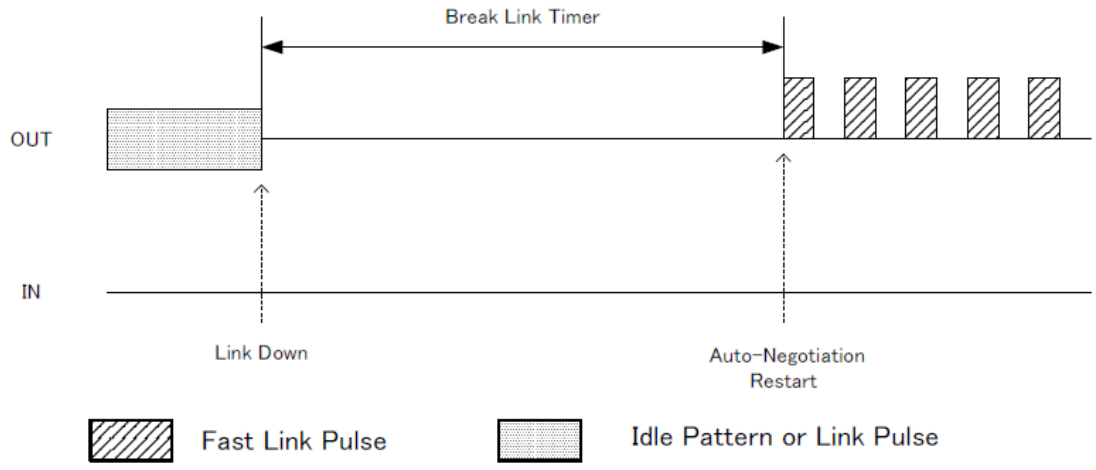
7.2.2 Quick auto-negotiation function

R-IN32M3-EC supports quick auto-negotiation function which means completing auto negotiation in less time than the specific time of IEEE802.3 and link up.

If the PHY is corresponding to the quick auto negotiation, Auto negotiation can be complete in a shorter time than normal by reducing the timer time of the three elements described below among the auto negotiation state machine.

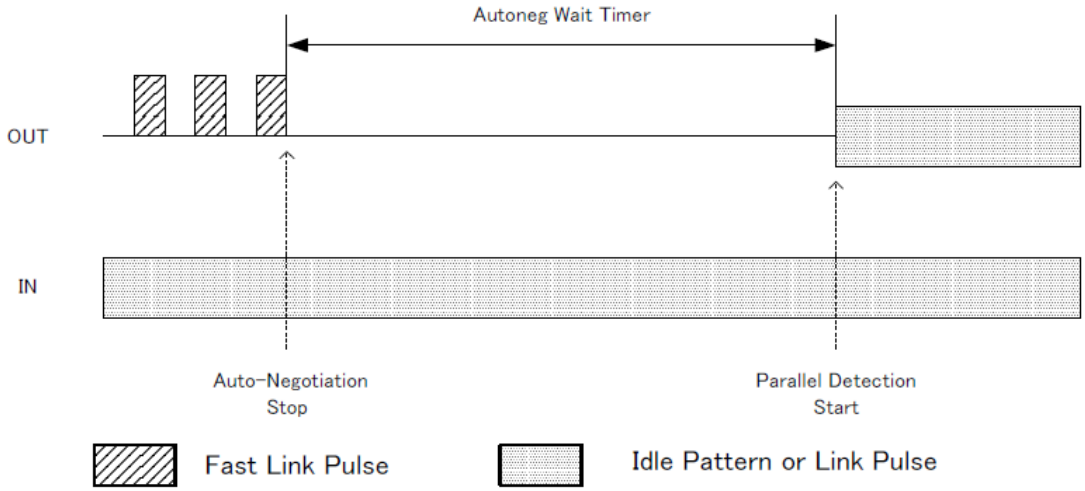
- Break Link Timer

Break Link Timer is defined as the time from PHY links down to auto-negotiation restarts and it is usually 1250ms.



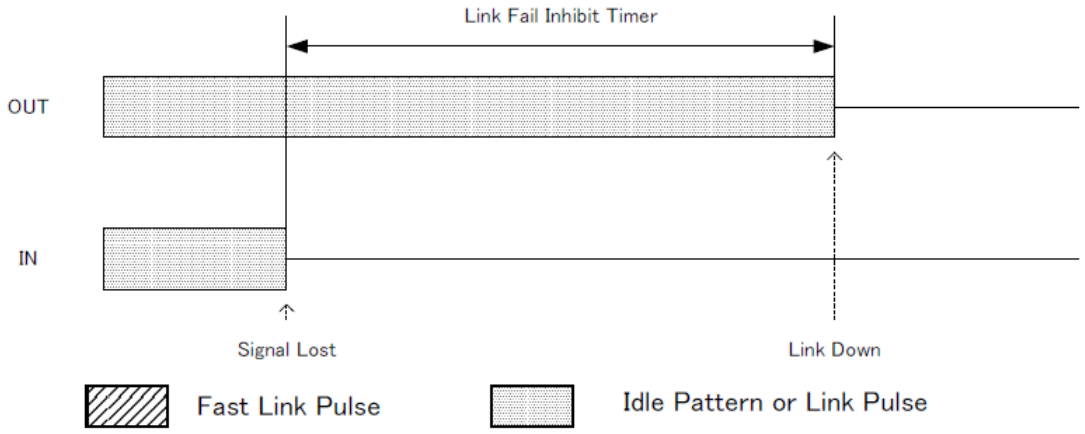
- Autonego Wait Timer

Autonego Wait Timer is defined as the waiting time from auto-negotiation stops to parallel detection starts and it is usually 850ms.



- Link Fail Inhibit Timer

Link Fail Inhibit Timer is defined as the waiting time from signal loss or becomes abnormal to link down and it is usually 850ms.



This three timer can be set by setting the 8-5 bit of register 18 (PHY_MODE[3:0] bit). When PHY_MODE[3] is 0, the value of PHY_MODE[1:0] can't be reflected. Please set PHY_MODE[3] 1 if you want to use this function.

PHY_MODE[3]	PHY_MODE[1:0]	Break Link Timer	Autoneg Wait Timer	Link Fail Inhibit Timer
0	XX	1250ms	850ms	850ms
1	00	80ms	35ms	50ms
1	01	120ms	50ms	75ms
1	10	240ms	100ms	150ms
1	11	1250ms	850ms	850ms

7.2.3 Cable diagnostic function (TDR function)

Cable diagnostic function (TDR function) is a diagnostic function for detecting the type and location of abnormality when disconnection or short occurs in the Ethernet cable. Output the pulse of Ethernet cable and measuring the time of pulse waveform reflected by the cable. This time can be used to determine the distance of abnormal whether the short or open from polarity.

The mechanism is as follows. ①is the test pulse in Figure 7.2, ②is the threshold for detecting the reflected pulse and can be set by register. When the cable is disconnected (cable end open), the sent pulse will get back attenuated in the same polarity as shown in Figure 7.2. When the cable is short-circuited (cable end closed), the sent pulse will get back attenuated in opposite phase as shown in Figure 7.3.

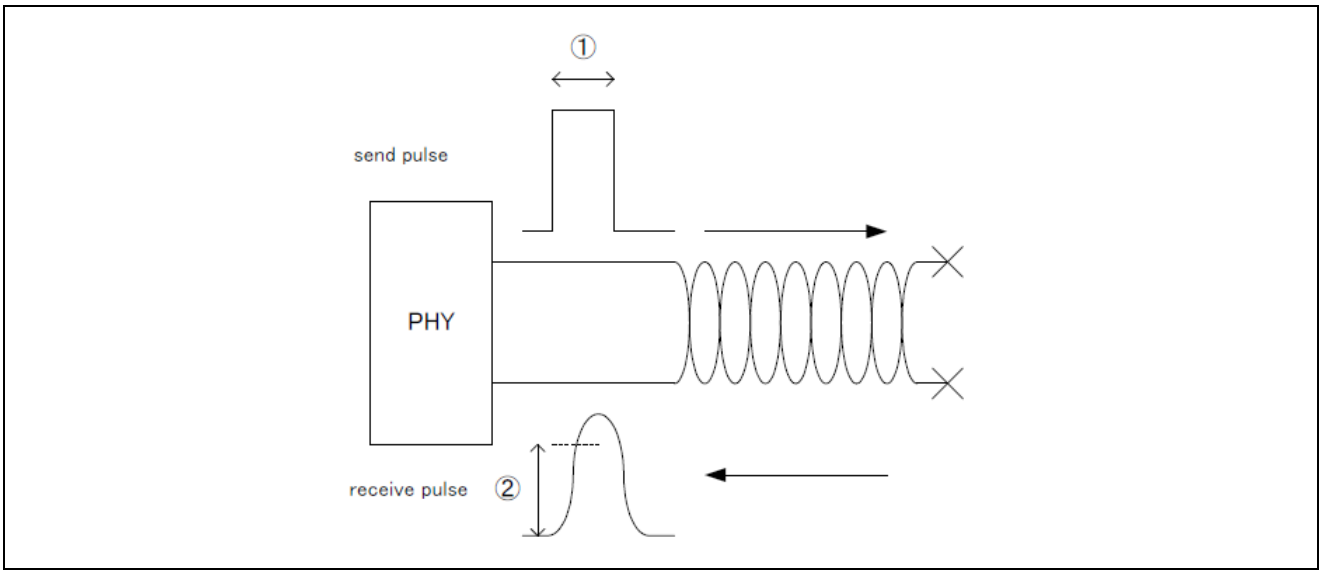


Figure 7.2 Behavior of cable disconnected

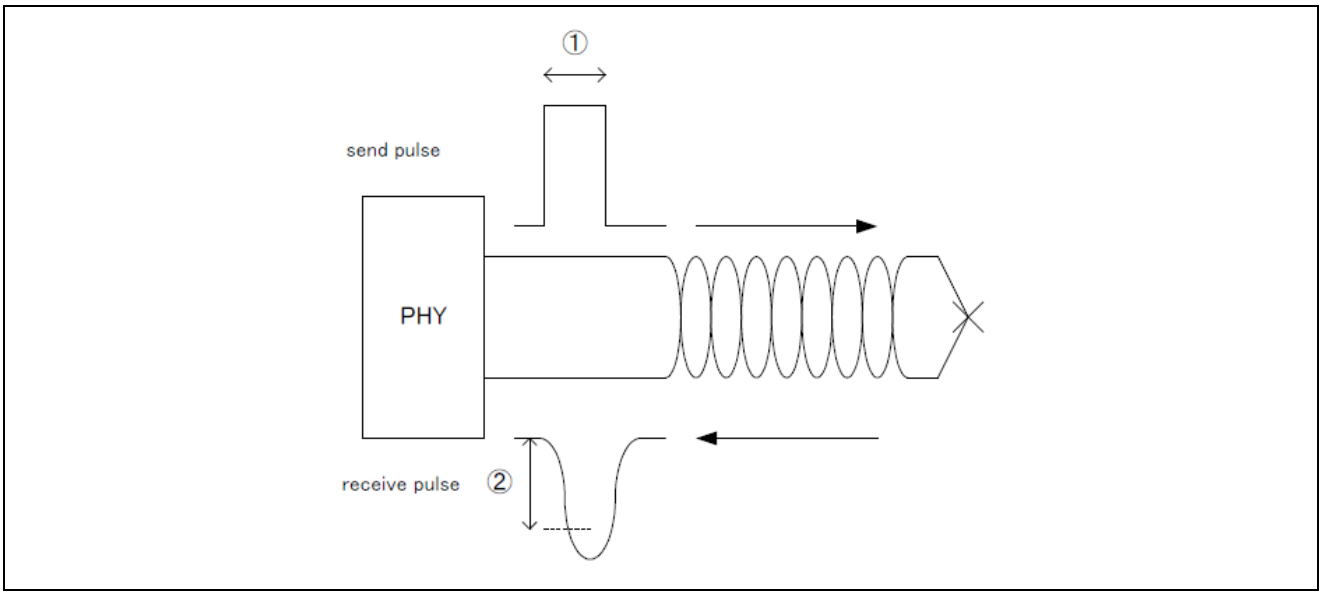


Figure 7.3 Behavior of cable short-circuited

The operation of TDR function is performed by using register 25 and register 26 as follows.
Disable the auto-negotiation and auto-crossover and set to 100Base-Half Duplex at first. It won't be measured correctly without this. Then, set the register with parameters related to pulse transmission and pulse detection whether TX line or RX line. Pulse is sent by writing 1 to the DIAG_INIT bit and the measurement is started after the configuration is complete.

The value of counter when pulse is detected is saved in DIAGCNT register and the information about open or short is saved in the DIAG_POL register at this time.
The following shows an example of setting the parameters when measuring. However, please note that it is necessary to adjust some parameters depending on the configuration of hardware and the installation environment.

No.	Cable length	ADC_TRIGGER	CNT_WINDOW	PW_DIAG	Conditions of counter value
1	Below 20m	10	15	2	DIAGCNT≠255 and DIAGCNT≦42
2	20m～40m	10	30	8	DIAGCNT≠255 and 32≦DIAGCNT≦68
3	40m～60m	8	50	8	DIAGCNT≠255 and 56≦DIAGCNT≦88
4	60m～80m	8	60	12	DIAGCNT≠255 and 78≦DIAGCNT≦114
5	More than 80m	8	75	12	DIAGCNT≠255 and 106≦DIAGCNT

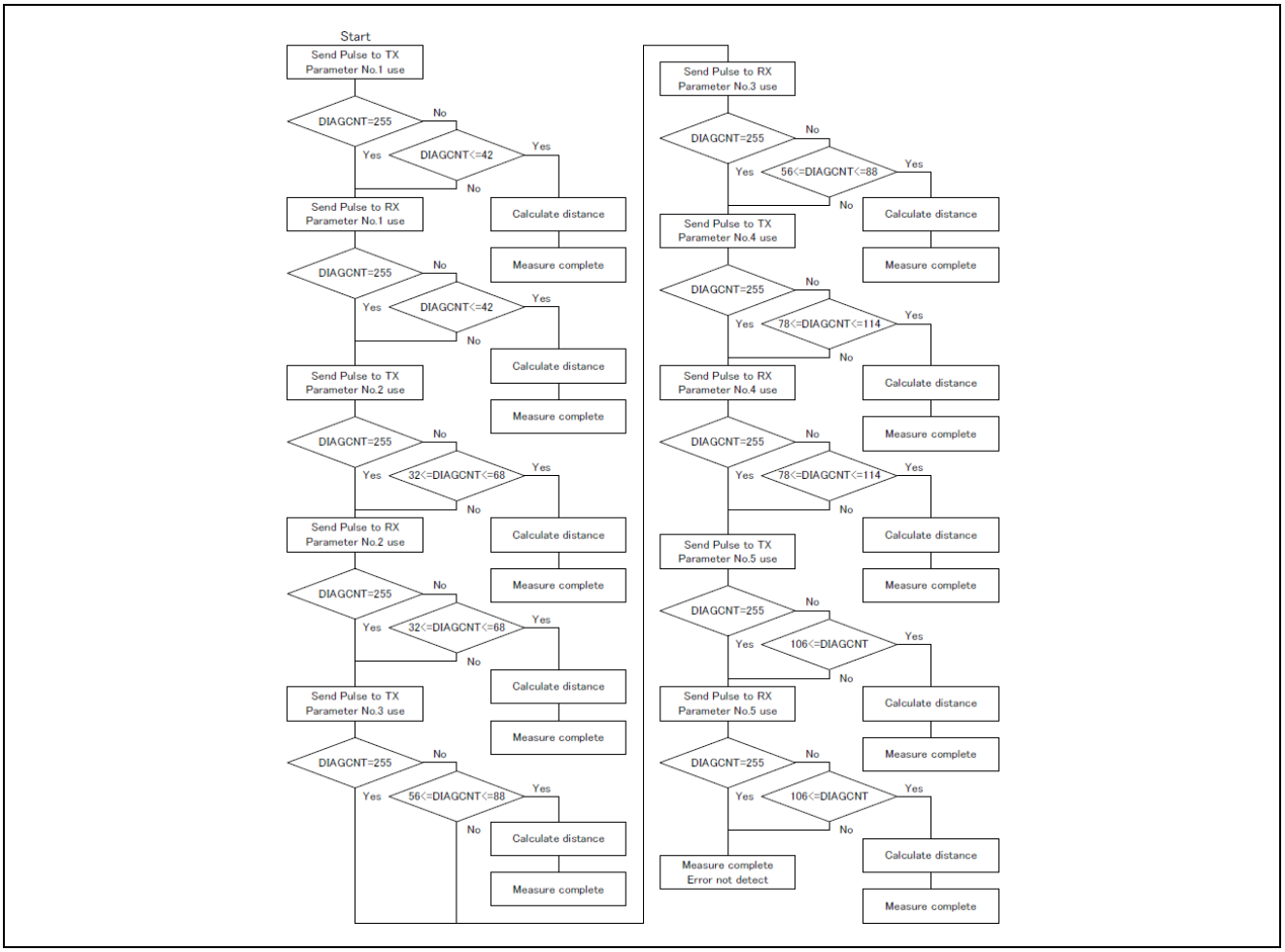


Figure 7.4 cable diagnostic process flow

7.2.4 Fast link-loss detection function

It is possible to generate the interrupt as soon as possible or bring down the link by monitoring the state of the communication when the communication is poor. It has two functions of BER monitor and FEQ monitor.

(1) BER monitor

Bit error rate (BER) function can be used to measure the bit error of specific time, count the number of errors and notify. When the threshold is exceeded, it can link down as a trigger and tell CPU with an interrupt. Element to be an error is when it is different between IDLE state and data communication as follows.

- In the IDLE state which communication is not performed, count the error judged as bit error when received symbol other than J which means the start of IDLE symbol or frame delimiter.
- When the communication is performed, count the error judged as bit error when received other than 32 kinds of symbol.

The operation of the BER monitor function is done by register 23 and as shown below.

The first step is to check whether the port is in link state by reading BER_LNK_OK. Pay attention on the link-down state which does not work properly. Set the BER_CNT_LNK_EN, BER_CNT_TRIG, BER_WINDOW parameters once the link state is verified. The error detection function starts to operate by writing a non-zero on BER_WINDOW. An interrupt is generated when the number of errors exceeds the threshold is detected within the specified time in the BER_WINDOW. When using the interrupt, please release the interrupt mask by writing 1 to bit 10 of register 30 before setting the parameters before. To end the operation of BER function, write 0 to BER_WINDOW. When using an interrupt, mask the interrupt by writing 0 to bit 10 of register 30.

(2) FEQ motor

To stably receive the incoming data, optimization is done by filtering the incoming signal by DSP in PHY. FEQ is the coefficients of this filter and the value fluctuates greatly when the amplitude of the signal being received is changed.

It can output the interrupt when detecting variation exceeds the threshold set in advance or link down by monitoring the variation.

The operation of FEQ monitor function is done by register 24 shown as below.

Firstly, set the variation to be detected in FEQ_DELTA. The reference value at the time of writing can be referred by writing 0xfffe to FEQ_DELTA and reading FEQ_VAL. FEQ monitor function will begin to work when the threshold of variable of FEQ_DELTA is set.

Current value of FEQ monitor can be detected by reading FEQ_VAL. An interrupt is generated when the value of FEQ_VAL exceeds the threshold. When using the interrupt, please release the interrupt mask by writing 1 to bit 9 of register 30 before setting the parameters before. To end the operation of FEQ function, write 0xFFFF to FEQ_DELTA. When using an interrupt, mask the interrupt by writing 0 to bit 9 of register 30.

7.3 power down mode

It has hardware power down mode, software power down mode and energy detection power mode and each of the power down modes is described as follows.

7.3.1 Hardware power down mode

It can be shifted to hardware power down mode by setting 1 to bit 2（P0PHYEN）or bit 5（P1PHYEN）of Ethernet PHY operation mode control register（PHYMD）. Ethernet PHY does not work at all in hardware power down mode and MII management register can't be accessed. The power consumption of the port will be almost 0. To wake up from the hardware power down mode, set 0 to bit 2（P0PHYEN）or bit 5（P1PHYEN）of Ethernet PHY operation mode control register（PHYMD）. When returning from the hardware power down mode, both analog and digital circuits are initialized by Ethernet PHY and so is MII management registers.

7.3.2 Software power down mode

It can be shifted to software power down mode by setting 1 to bit 11（POWERDOWN）of MII management register 0 with Ethernet PHY internal. IDLE signal is not output in the transition of software power down mode and in software power down mode but MII management register can be accessed and controlled in software power down mode. To wake up from the software power down mode, set 0 to bit 11（POWERDOWN）of MII management register 0. The digital circuits are initialized automatically by Ethernet PHY at the conclusion of software power down mode. However, please note that some bits of MII management registers are not initialized. Bit described as "NASR" are eligible in 7.4 MII management register with Ethernet PHY internal.

7.3.3 Energy detection power down mode

It can be shifted to energy detection power down mode by setting 1 to bit 13（EDPWRDOWN）of MII management register 17 with Ethernet PHY internal. Please note that energy detection power down mode can't be transited to when auto-negotiation is enabled. In this mode, Ethernet PHY will not output anything except for several modules such as serial management interface when there is no input of link pulse or packet signal to Ethernet PHY. Ethernet PHY will be reset automatically to the speed before becoming energy detection power down mode when link pulse or packet signal is input in this state. At that time, you may fail to receive the first and the next signal because of the detection of link pulse and packet signal.

Set 0 to bit 13（EDPWRDOWN） of MII management register to end the energy detection power down mode and return to the normal mode.

7.4 MII management register with Ethernet PHY internal

It is the MII management register includes Ethernet PHY. The state of Ethernet PHY can be got by various settings to the Ethernet PHY. This register can be accessed by either the MIIM register of on-chip Ethernet MAC or MII Management Interface register of EtherCAT Slave Controller via the serial management interface from each MAC.

Caution Register 8-15 are the mirror of register 24-31 and the entity of register 8-15 do not exit. Access to register 8-15 is prohibited.

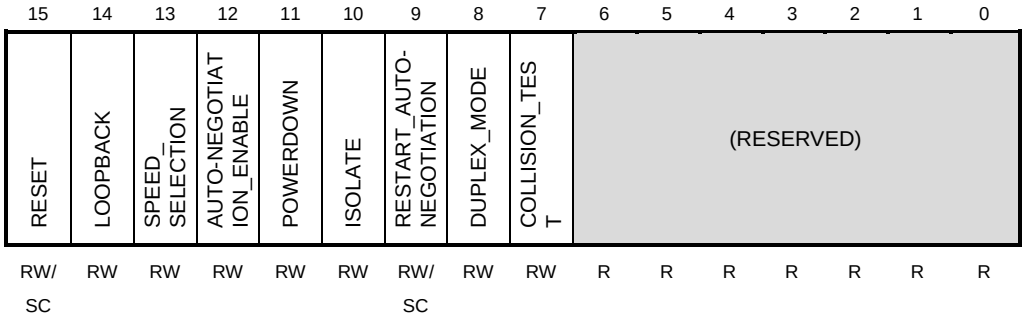
Table 7.1 Summary of PHY MII Management registers

Register address	Register name	type
0	Control Register	Basic
1	Status Register	Basic
2	PHY Identifier	Extension
3	PHY Identifier	Extension
4	Auto-Negotiation Advertisement Register	Extension
5	Auto-Negotiation Link Partner Ability Register	Extension
6	Auto-Negotiation Expansion Register	Extension
7	Auto-Negotiation Next Page Transmit Register	Extension
8	Unsupported(Access prohibited for the mirror of register 24)	–
9	Unsupported (Access prohibited for the mirror of register 25)	–
10	Unsupported (Access prohibited for the mirror of register 26)	–
11	Unsupported (Access prohibited for the mirror of register 27)	–
12	Unsupported (Access prohibited for the mirror of register 28)	–
13	Unsupported (Access prohibited for the mirror of register 29)	–
14	Unsupported (Access prohibited for the mirror of register 30)	–
15	Unsupported (Access prohibited for the mirror of register 31)	–
16	Silicon Revision Register	Vendor-specific
17	Mode Control/Status Register	Vendor-specific
18	Special Mode Register	Vendor-specific
19	Reserved	Vendor-specific
20	Reserved	Vendor-specific
21	Reserved	Vendor-specific
22	Reserved	Vendor-specific
23	BER counter Register	Vendor-specific
24	FEQ monitor Register	Vendor-specific
25	Diagnostic control/Status Register	Vendor-specific
26	Diagnostic Counter Register	Vendor-specific
27	Special Control/Status Indication Register	Vendor-specific
28	Reserved	Vendor-specific
29	Interrupt Factor Register	Vendor-specific
30	Interrupt Factor Mask Register	Vendor-specific
31	PHY Special Control/Status Register	Vendor-specific

7.4.1 Register 0 - Control Register

Register 0 makes the basic settings of the Ethernet PHY.

MR0



PHY Address 00H
Initial Value 1000H

Bit Position	Bit Name	Function
15	RESET	Reset the Ethernet PHY. Please don't change the settings of the other bits of this register when resetting. 0 : Normal operation 1 : Software Reset
14	LOOPBACK	Enable/Disable the settings of internal loop-back mode 0 : Disable 1 : Enable
13	SPEED_SELCTION	Set the Link speed 0 : 10Mb/s 1 : 100Mb/s
12	AUTO-NEGOTIATION_ ENABLE	Enable/Disable the settings of auto-negotiation 0 : Disable 1 : Enable
11	POWERDOWN	Set the power down mode 0 : Normal operation 1 : Power down mode
10	ISOLATE	Set isolation 0 : Normal operation 1 : Electrically disconnect from MII
9	RESTART_ AUTO-NEGOTIATION	Restart the auto negotiation process 0 : Normal operation 1 : Restart the auto negotiation process
8	DUPLEX_MODE	Set the duplex mode. This setting is invalid when bit 12 is 1 0 : Half Duplex 1 : Full Duplex
7	COLLISION_TEST	Enable/Disable the settings of collision signal 0 : Disable 1 : Enable
6-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.2 Register 1 – Status Register

Register 1 shows the status of Ethernet PHY.

MR1

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
100BASE-T4	100BASE-TX_ FULL_DUPLEX	100BASE-TX_ HALF_DUPLEX	10M_FULL_ DUPLEX	10M_HALF_ DUPLEX	(RESERVED)					AUTO-NEGOTIOATIO N_COMPLETE	REMOTE_FAULT	AUTO-NEGOTIOATIO N_ABILITY	LINK_STATUS	JABBER_DETECT	EXTENDED_ CAPABILITY
R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R/LL	R/LH	R

PHY Address 01H

Initial Value 7809H

Bit Position	Bit Name	Function
15	100BASE-T4	Shows enable/disable on communication of 100BASE-T4 0 : Disable 1 : Enable
14	100BASE-TX_ FULL_DUPLEX	Shows enable/disable on full duplex communication of 100BASE-TX 0 : Disable 1 : Enable
13	100BASE-TX_ HALF_DUPLEX	Shows enable/disable on half duplex communication of 100BASE-TX 0 : Disable 1 : Enable
12	10M_FULL_DUPLEX	Shows enable/disable on 10Mb/s full duplex communication 0 : Disable 1 : Enable
11	10M_HALF_DUPLEX	Shows enable/disable on 10Mb/s half duplex communication 0 : Disable 1 : Enable
10-6	(RESERVED)	Reserved (Write 0 and ignore reading)
5	AUTO-NEGOTIATION_ COMPLETE	Notice of auto negotiation completion 0 : Incompletion 1 : Completion
4	REMOTE_FAULT	Shows the detection result of the failure of remote side. 0 : Failure undetected 1 : Failure detected
3	AUTO-NEGOTIATION_ ABILIT	Enable/Disable the settings of auto-negotiation 0 : Disable 1 : Enable
2	LINK_STATUS	Shows the status of link 0 : link down 1 : link up
1	JABBER_DETECT	Shows the detection result of jabber state 0 : Jabber undetected 1 : Jabber detected
0	EXTENDED_ CAPABILITY	Shows whether the extended register is used 0 : Use only basic register set 1 : Use extended register set

7.4.3 Register 2, 3 - PHY Identifier

Register 2, 3 shows the identification number of PHY by 32-bit in total.

MR2

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ID_NUMBER															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address 02H
Initial value 0033H

Bit Position	Bit Name	Function
15-0	PHY_ID_NUMBER	3rd to 18th bit of OUI

MR3

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PHY_ID_NUMBER						MODEL_NUMBER						REVISION_NUMBER			
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address 03H
Initial value 2002H

Bit Position	Bit Name	Function
15-10	PHY_ID_NUMBER	19th to 24th bit of OUI
9-4	MODEL_NUMBER	Manufacturer model number
3-0	REVISION_NUMBER	Manufacturer revision number

7.4.4 Register 4 - Auto-Negotiation Advertisement Register

Register 4 inform the partner when using auto negotiation mode.

MR4

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	(RESERVED)	REMOTE_FAULT	(RESERVED)	PAUSE_OPERATION		100BASE-T4	100BASE-TX_FULL_DUPLEX	100BASE-TX	10BASE-T_FULL_DUPLEX	10BASE-T	SELECTOR_FIELD				
RW	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW

PHY Address
04H
Initial value
01E1H

Bit Position	Bit Name	Function
15	NEXT_PAGE	Support Next Page function or not 0：Not supported 1：Supported
14	(RESERVED)	Reserved (Write 0 and ignore reading)
13	REMOTE_FAULT	Set the status of local device in remote fault detection function 0：Not fault 1：Fault
12	(RESERVED)	Reserved (Write 0 and ignore reading)
11-10	PAUSE_OPERATION	Set the action of Pause 00：No action 01：Symmetry Behavior 10：Asymmetry Behavior to the link partner 11：Asymmetry Pause Behavior to Symmetry pulse and local device
9	100BASE-T4	100BASE-T4 supported or not (Fixed to 0 in this LSI) 0：Not supported 1：Supported
8	100BASE-TX_ FULL_DUPLEX	100BASE-TX Full Duplex supported or not 0：Not supported 1：Supported
7	100BASE-TX	100BASE-TX supported or not 0：Not supported 1：Supported
6	10BASE-T_ FULL_DUPLEX	10BASE-T Full Duplex supported or not 0：Not supported 1：Supported
5	10BASE-T	10BASE-T supported or not 0：Not supported 1：Supported
4-0	SELECTOR_FIELD	00001：IEEE std 802.3

7.4.5 Register 5 - Auto-Negotiation Link Partner Ability (Base Page) Register

Register 5 shows the Base Page of the information received from the partner when using auto negotiation.

MR5 (Base Page)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	ACKNOWLEDGE	REMOTE_FAULT	(RESERVED)		PAUSE_OPERATION	100BASE-T4	100BASE-TX_FULL_DUPLEX	100BASE-TX	10BASE-T_FULL_DUPLEX	10BASE-T	SELECTOR_FIELD				
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address 05H Initial value 0001H

Bit Position	Bit Name	Function
15	NEXT_PAGE	Whether there are additional pages 0：Last page 1：Have additional pages
14	ACKNOWLEDGE	Result of link signal from the link partner 0：Failure Success 1：Success
13	REMOTE_FAULT	Fault condition of the link partner 0：Not fault 1：Fault
12-11	(RESERVED)	Reserved (Write 0 and ignore reading)
10	PAUSE_OPERATION	Pause auction of MAC of remote device supported or not 0：Not supported 1：Supported
9	100BASE-T4	100BASE-T4 supported or not (Fixed to 0 in this LSI) 0：Not supported 1：Supported
8	100BASE-TX_ FULL_DUPLEX	100BASE-TX Full Duplex supported or not 0：Not supported 1：Supported
7	100BASE-TX	100BASE-TX supported or not 0：Not supported 1：Supported
6	10BASE-T_ FULL_DUPLEX	10BASE-T Full Duplex supported or not 0：Not supported 1：Supported
5	10BASE-T	10BASE-T supported or not 0：Not supported 1：Supported
4-0	SELECTOR_FIELD	00001：IEEE std 802.3

7.4.6 Register 5 – Auto-Negotiation Link Partner Ability (Next Page) Register

Register 5 shows the Next Page of the information received from the partner when using auto negotiation.

MR5 (Next Page)

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	ACKNOWLEDGE	MESSAGE_PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE_UNFORMATTED_CODE_FIELD										
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address 05H
Initial value 0000H

Bit Position	Bit Name	Function
15	NEXT_PAGE	Whether there are additional Next page 0：Last page 1：Have additional Next Page
14	ACKNOWLEDGE	Result of link signal from the link partner 0：Success 1：Failure
13	MESSAGE_PAGE	Encoding method of bit 10-0's code filed 0：Unformatted Page 1：Message Page
12	ACKNOWLEDGE2	Shows correspondence to message supported or not 0：Not supported 1：Supported
11	TOGGLE	Used for synchronization with the link partner during the replacement with Next Page. 0：Sent link code word is 1 1：Sent link code word is 0
10-0	MESSAGE_UNFORMATTED_CODE_FIELD	11-bit code word received from the link partner

7.4.7 Register 6- Auto-Negotiation Expansion Register

MR6

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)											PARALLEL_ DETECTION_FAULT	LINK_PATTNER_ NEXT_PAGE_ABLE	NEXT_PAGE_ABLE	PAGE_RECEIVED	LINK_PARTNER_AU TO-NEGOTIATION_ ABLE
R	R	R	R	R	R	R	R	R	R	R	R/LH	R	R	R/LH	R

PHY Address
06H
Initial Value
0004H

Bit Position	Bit Name	Function
15-5	(RESERVED)	Reserved (Write 0 and ignore reading)
4	PARALLEL_ DETECTION_FAULT	Shows whether the failure was detected in parallel detection function. It is set to 0 when reading register 6 0：Undetected 1：Detected
3	LINK_PATNER_ NEXT_PAGE_ABLE	Next Page function of link partner supported or not 0：Not supported 1：Supported
2	NEXT_PAGE_ABLE	Next Page function of local device supported or not 0：Not supported 1：Supported
1	PAGE_RECEIVED	Receive new link code word and stored in register 5. And it turns to 0 when reading register 6. 0：New page not received 1：New page received
0	LINK_PATNER_ AUTO-NEGOTIATION_ ABLE	Auto negotiation with link partner supported or not 0：Not supported 1：Supported

7.4.8 Register 7 - Auto-Negotiation Next Page Transmit Register

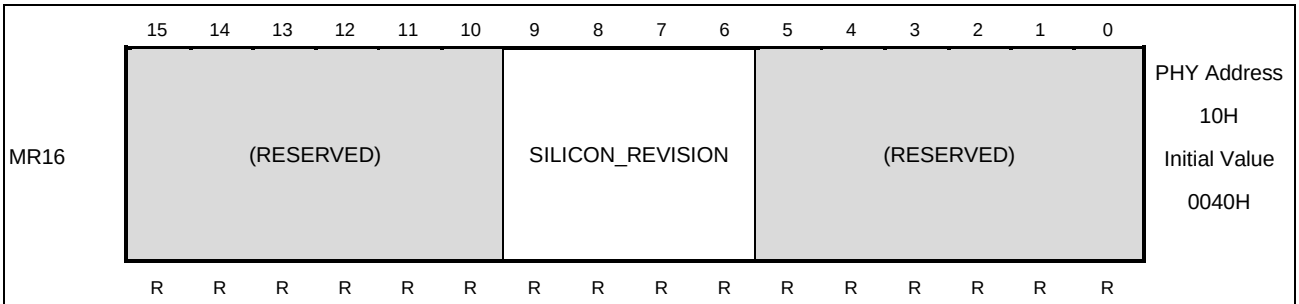
MR7

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NEXT_PAGE	(RESERVED)	MESSAGE_PAGE	ACKNOWLEDGE 2	TOGGLE	MESSAGE_UNFORMATTED_CODE_FIELD										
RW	R	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PHY Address
07H
Initial Value
2001H

Bit Position	Bit Name	Function
15	NEXT_PAG	Whether there are additional Next page 0：Last page 1：Have additional Next Page
14	(RESERVED)	Reserved (Write 0 and ignore reading)
13	MESSAGE_PAGE	Encoding method of bit 10's code field 0：Unformatted Page 1：Message Page
12	ACKNOWLEDGE2	Shows correspondence to message supported or not 0：Not supported 1：Supported
11	TOGGLE	Used for synchronization with the link partner during the replacement with Next Page. 0：Sent link code word is 1 1：Sent link code word is 0
10-0	MESSAGE_UNFORMATTED_CODE_FIELD	11-bit code word send to the link partner

7.4.9 Register 16- Silicon Revision Register


15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MR16
(RESERVED)
SILICON_REVISION
(RESERVED)
PHY Address
10H
Initial Value
0040H
R R R R R R R R R R R R R R R R

Bit Position	Bit Name	Function
15-10	(RESERVED)	Reserved (Write 0 and ignore reading)
9-6	SILICON_REVISION	Shows silicon revision
5-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.10 Register 17- mode control/status Register

(1/2)

MR17

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)	FASTRIP	EDPWRDOWN	(RESERVED)	LOWSQEN	(RESERVED)	FARLOOPBACK	FASTEST	AUTOMDIX_EN	MDI_MODE	(RESERVED)	DCD_PAT_GEN	(RESERVED)	FORCE_GOOD_LINK_STATUS	ENERGYON	(RESERVED)
RW	RW, NASR	RW	RW	RW	RW	RW	RW	RW	RW	R	RW	RW	RW	R	RW

PHY Address
11H
Initial Value
0080H

Bit Position	Bit Name	Function
15	(RESERVED)	Reserved (Write 0 and ignore reading)
14	FASTRIP	Set 10BASE-T fast mode. Only simulation can be used. 0：Normal operation 1：PHYT_10 test mode
13	EDPWRDOWN	Enable/disable the settings of power down mode for energy detection 0：Disabled 1：Enabled
12	(RESERVED)	Reserved (Write 0 and ignore reading)
11	LOWSQEN	Low squelch setting 0：Normal operation 1：Low down the threshold(Increase sensitivity of signal)
10	(RESERVED)	Reserved (Write 0 and ignore reading)
9	FARLOOPBACK	Enable/disable the settings of remote loopback mode. All the packets are send back at the same time by setting. Only correspond to 100BASE-TX/FX mode. 0：Disabled 1：Enabled
8	FASTEST	Enable/disable the settings of test mode of auto negotiation. Only used for simulation. The time of software reset is also decreased. 0：Disabled 1：Enabled
7	AUTOMDIX_EN	Enable/disable the settings of auto-MDIX function 0：Disabled(Set bit 6 of register 17 manually) 1：Enabled
6	MDI_MODE	Set the MDI/MDI-X mode manually when bit 7 of register 17 is 0. If bit 7 of register 17 is 1, it means the status of mode and write to the register is disabled at this time. 0：MDI mode 1：MDI-X mode
5	(RESERVED)	Reserved (Write 0 and ignore reading)

(2/2)

Bit Position	Bit Name	Function
4	DCD_PAT_GEN	Enable/disable the settings of pattern generation for DCD measurement in the test mode. 0：Disabled 1：Enabled
3	(RESERVED)	Reserved (Write 0 and ignore reading)
2	FORCE_GOOD_ LINK_STATUS	Make the link state in force. Only use for test. 0：Normal operation 1：Link status of 100BASE-X
1	ENERGYON	Shows the energy detection state of line. 0：Energy from the line within 256ms is not detected. 1：Detection of energy from the line.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.11 Register 18- Special mode register

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
MR18	(RESERVED)					FX_MODE	(RESERVED)	PHY_MODE[3:0]				PHY_ADD[4:0]					PHY Address 12H Initial Value 00E0H
	RW	R	R	RW	RW	RW NASR	RW	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	RW NASR	

Bit Position	Bit Name	Function
15-11	(RESERVED)	Reserved (Write 0 and ignore reading)
10	FX_MODE	Enable/Disable setting in 100BASE-FX mode. When enable the 100BASE-FX mode, PHY_MODE(Bit 8-5 of register 18) must be 0011 or 0010. 0：Invalid (10BASE-T/100BASE-TX mode) 1：Valid
9	(RESERVED)	Reserved (Write 0 and ignore reading)
8-5	PHY_MODE[3:0]	Set PHY operate mode.

PHY_MODE [3:0]	Speed	Duplex	Auto negotiation
0000	10BASE-T	Half duplex	Invalid
0001	10BASE-T	Duplex	Invalid
0010	100BASE-TX/FX	Half duplex	Invalid. Enable CRS of sending and receiving.
0011	100BASE-TX/FX	Duplex	Invalid. Enable CRS of sending.
0100	100BASE-T	Half duplex	Valid. Enable CRS of sending and receiving.
0101	100BASE-T Repeater mode	Half duplex	Valid. Enable CRS of receiving.
0110	PowerDown Mode (For testing)	-	-
0111	All	Both sides	Valid
1000	All	Full duplex Force by parallel detection	Enable quick auto negotiation. Select timing by bit 1 and bit 0[Note 1].
1001			
1010			
1011			
1100		Half-duplex by parallel detection(standard)	
1101			
1110			
1111	Loopback/Isolate	-	- (Internal loop-back mode)

4-0	PHY_ADD[4:0]	Specify the PHY address. Setting of PHY_ADD[0] is ignored and 0 is assigned to port 0 while 1 to port 1.

Note 1 The timing of auto-negotiation can be changed in order to reduce the auto-negotiation time between 2 PHY. It is possible to adjust the timing by changing the settings when link problem appears.

PHY_MODE[3]	PHY_MODE[1:0]	Break Link Timer	Autoneg Wait Timer	Link Fail Inhibit Timer
0	XX	1250ms	850ms	850ms
1	00	80ms	35ms	50ms
1	01	120ms	50ms	75ms
1	10	240ms	100ms	150ms
1	11 (IEEE compliant)	1250ms	850ms	850ms

7.4.12 Register 19-Reserved

MR19

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)															
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address
13H
Initial Value
0000H

Bit Position	Bit Name	Function
15-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.13 Register 20 – Reserved

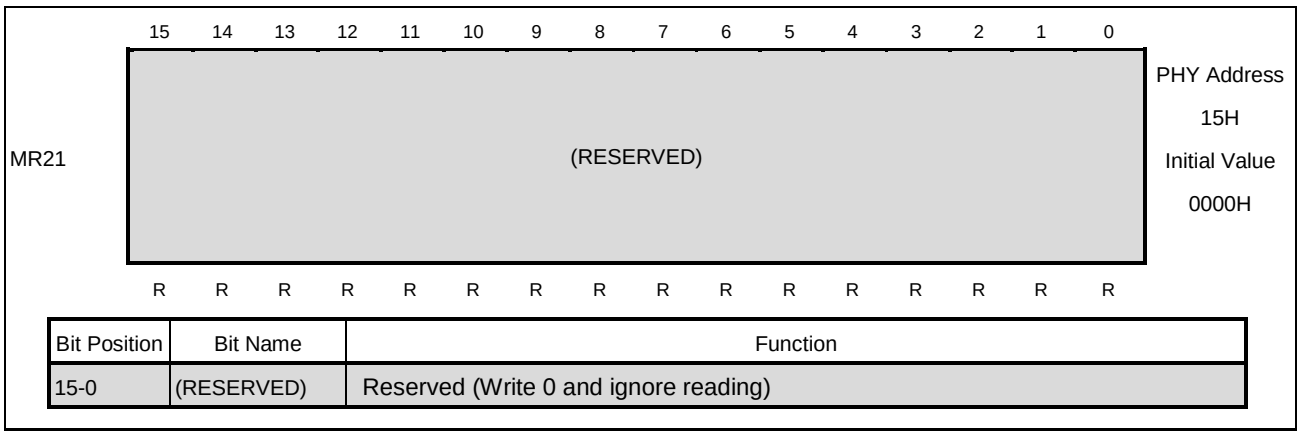
MR20

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PHY Address
14H
Initial Value
0000H

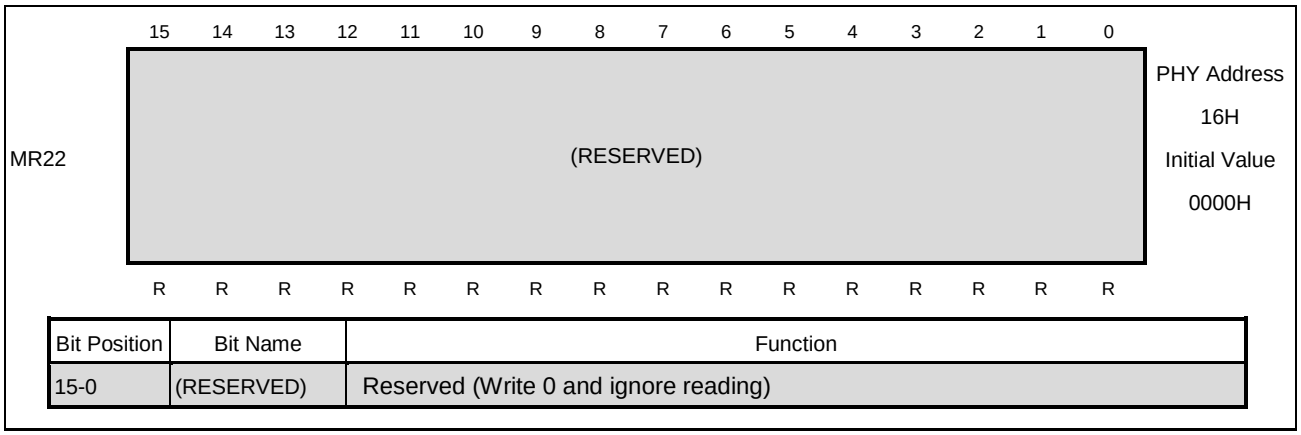
Bit Position	Bit Name	Function
15-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.14 Register 21 – Reserved



Bit Position	Bit Name	Function
15-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.15 Register 22 – Reserved



Bit Position	Bit Name	Function
15-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.16 Register 23-BER counter Register

Set BER counter function mode of Ethernet PHY and show the results.

MR23

15	14	13 12 11	10 9 8 7	6 5 4 3 2 1 0
BER_LNK_OK	BER_CNT_LNK_EN	BER_CNT_TRIG	BER_WINDOW	BER_COUNT
R	RW	RW RW RW	RW RW RW RW	R R R R R R R

PHY Address 17H
Initial Value 5080H

Bit Position	Bit Name	Function
15	BER_LNK_OK	Shows the quality status of the link. It turns to 1 if the value of BER counter is below the threshold after startup. It is used to detect the reliable links after startup. 0：Not linked or the state of the link is not good. 1：The state of the link is good.
14	BER_CNT_LNK_EN	Operation when the count value of BER and FEQ monitor exceeds the threshold. 0：Only BER_LNK_OK becomes 0 without bringing down the link. 1：Bring down the link.
13-11	BER_CNT_TRIG	Set the condition to determine the link down or interrupt occurrence by the value of BER counter. 0：1 or more 1：More than 1(2 or more) 2：More than 2(3 or more) 3：More than 4(5 or more) 4：More than 8(9 or more) 5：More than 16(17 or more) 6：More than 32(33 or more) 7：More than 64(65 or more)
10-7	BER_WINDOW	Set the width of the window of BER counter. 1：0.2 ms 2：0.4 ms 3：0.8 ms … 15：3.2 sec
6-0	BER_COUNT	Count value of bit errors in the window time before current.

7.4.17 Register 24-FEQ monitor Register

Set FEQ monitor function Ethernet PHY and show the results.

MR24

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
FEQ_DELTA / FEQ_VAL															
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW

PHY Address
18H
Initial Value
0000H

Bit Position	Bit Name	Function
15-0	FEQ_DELTA (Write)	Set the amount of change in FEQ2 factor allowed for the value of the reference that has been latched. When BER_CNT_LINK_EN bit of register 23 is 1, if the value of FEQ2 exceeds this value, FEQ interrupt is generated and the link is down. FFFF：Disable FEQ monitor function and continue to latch on the FEQ2 factor ongoing. FFFE：The current reference value can be read from this register. The value of FEQ_DELTA does not change. Other: Set the threshold of amount of change. FEQ monitor function starts to work with setting this value.
	FEQ_VAL (Read)	Shows 17-2 bit of FEQ2 coefficient latched as a reference when write FFFE to FEQ_DELTA. Others: Current FEQ2 coefficient.

7.4.18 Register 25-Diagnostic control/Status Register

Set diagnostic function of Ethernet PHY and show the results.

MR25

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)	DIAG_INIT	ADC_MAX_VALUE / ADC_TRIGGER						DIAG_DONE	DIAG_POL	DIAG_SEL_LINE	PW_DIAG				
RW	RW/SC	RW	RW	RW	RW	RW	RW	R	R	RW	RW	RW	RW	RW	RW

PHY Address 19H
Initial Value 0000H

Bit Position	Bit Name	Function
15	(RESERVED)	Reserved (Write 0 and ignore reading)
14	DIAG_INIT	Start TDR test and generate a single cycle pulse. 0：Normal operation 1：Pulse generation (Turns to 0 after pulse generation)
13-8	ADC_MAX_VALUE (Read)	Shows the maximum/minimum signed value of the reflected wave. When the TDR test starts, PHY sends out a trigger pulse and waits for the reflected wave for 255 cycles (2040ns) of 8ns clock. DIAG_DONE bit is set after the time. Indicates the maximum value of the received wave if it is a positive value and minimum value if negative.
	ADC_TRIGGER (Write)	Sets the threshold voltage for detecting the reflected wave from 000111(0.5V) to 001111(1.5V). This setting cannot be read.
7	DIAG_DONE	Shows that the counter is stopped. 0：Running or TDR untested 1：Stop(set to 0 after reading)
6	DIAG_POL	Shows the polarity of the reflected wave detected. 0：Positive logic 1：Negative logic
5	DIAG_SEL_LINE	Select the line to implement the TDR test. 0：RX line 1：TX line
4-0	PW_DIAG	Set the width of the pulse send out at TDR test in range of 8ns to 248ns for each 8ns. 0：Normal operation Other than 0：Setting × 8 ns

7.4.19 Register 26-Diagnostic counter register

Set diagnostic counter of Ethernet PHY and show the results.

MR26

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CNT_WINDOW								DIAGCNT							
RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R	R	R	R

PHY Address
1AH
Initial Value
0000H

Bit Position	Bit Name	Function
15-8	CNT_WINDOW	Set the time to mask as invalid detection result from the start of delivery of the pulse. Set in order to avoid the influence of noise of the sent pulse itself and immediately after delivery. It will be about 0.8m per 1 count.
7-0	DIAGCNT	Shows the value of the counter when detecting reflected wave. It turns to 0x00 immediately after sending a pulse and 0xFF when the reflected wave is not detected. It becomes to 0x01 if the cable is not connected.

7.4.20 Register 27-Special control/Status instruction register

Set PHY mode of Ethernet PHY and show the results.

MR27

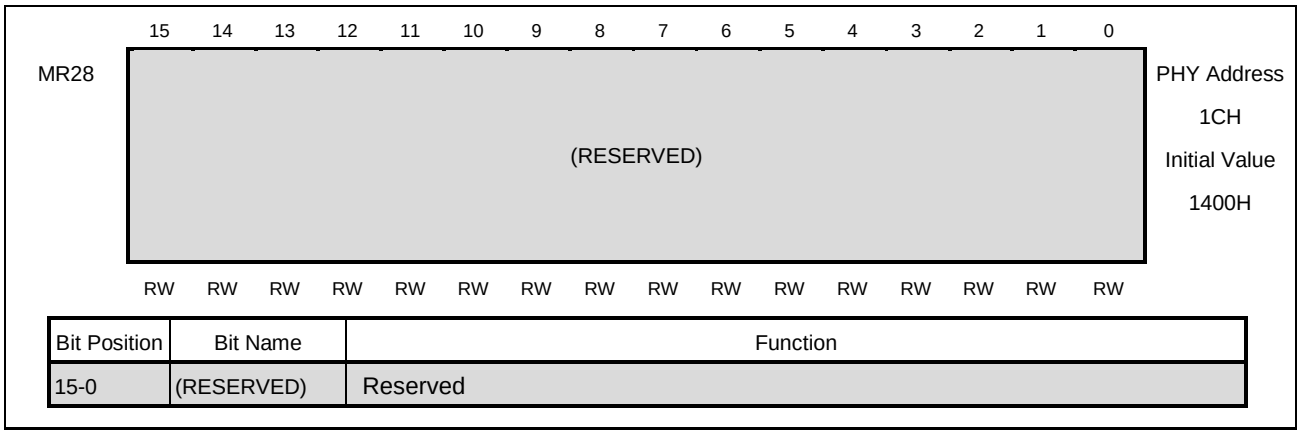
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			SWRST_FAST	SQEOFF	(RESERVED)					FEFIEN	XPOL	(RESERVED)			
RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	RW	R	R	R	R	R
				NASR											

PHY Address
1BH
Initial Value
0001H

Bit Position	Bit Name	Function
15-13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	SWRST_FAST	Test the software reset counter 0：Normal operation 1：Shorten the software reset counter from 256us to 10us(for production test)
11	SQEOFF	Valid/Invalid the SQE test 0：Valid 1：Invalid
10-6	(RESERVED)	Reserved (Write 0 and ignore reading)
5	FEFIEN	Valid/Invalid the setting of Far End Fault Indication in 100BASE-FX 0：Invalid 1：Valid
4	XPOL	Automatic polarity detection result of 10BASE-T 0：Normal 1：Reversal
3-0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.21 Register 28 – Reserved

This register is used for testing. Please don't read or write to this register.



Bit Position	Bit Name	Function
15-0	(RESERVED)	Reserved

7.4.22 Register 29- Interrupt Factor Register

Register 29 indicates the source of interrupt when the interrupt output of Ethernet PHY is active. Bit 1 points to the cause of the interrupt. Interrupt output is cleared by reading.

MR29

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			INT12	INT11	INT10	INT9	(RESERVED)	INT7	INT6	INT5	INT4	INT3	INT2	INT1	(RESERVED)
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

PHY Address
1DH
Initial Value
0000H

Bit Position	Bit Name	Function
15-13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	INT12	Clipping
11	INT11	Maxlvl
10	INT10	BER counter trigger
9	INT9	FEQ Trigger
8	(RESERVED)	Reserved (Write 0 and ignore reading)
7	INT7	Energy detection of the line
6	INT6	Auto-negotiation is complete
5	INT5	Remote fault detection
4	INT4	Link down
3	INT3	Auto-negotiation is complete and receive the last FLP
2	INT2	Parallel detection failure
1	INT1	Auto-negotiation is transition to Complete Acknkowledge state.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.23 Register 30-Interrupt Factor Mask Register

Enable/disable interrupt factors of Ethernet PHY. 0 is invalid (mask), while 1 is valid.

MR30

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			INT12_MASK	INT11_MASK	INT10_MASK	INT9_MASK	(RESERVED)	INT7_MASK	INT6?MASK	INT5_MASK	INT4_MASK	INT3_MASK	INT2_MASK	INT1_MASK	(RESERVED)
R	R	R	RW	RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R

PHY Address
1EH
Initial Value
0000H

Bit Position	Bit Name	Function
15-13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	INT12_MASK	Clipping
11	INT11_MASK	Maxlvl
10	INT10_MASK	BER counter trigger
9	INT9_MASK	FEQ trigger
8	(RESERVED)	Reserved (Write 0 and ignore reading)
7	INT7_MASK	Energy detection of the line
6	INT6_MASK	Auto-negotiation is complete
5	INT5_MASK	Remote fault detection
4	INT4_MASK	Link down
3	INT3_MASK	Auto-negotiation is complete and receive the last FLP
2	INT2_MASK	Parallel detection failure
1	INT1_MASK	Auto-negotiation is transition to Complete Acknkowledge state.
0	(RESERVED)	Reserved (Write 0 and ignore reading)

7.4.24 Register 31- PHY special control/Status register

Register 31 does the configuration and status of the special features of Ethernet PHY.

MR31

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
(RESERVED)			AUTODONE	(RESERVED)					ENABLE_4B5B	(RESERVED)	SPEED_ INDICATION			RX_DV_J2T	SCRAMBLE_ DISABLE
RW	RW	RW	R	RW	RW	RW	RW	RW	RW	RW	R	R	R	RW	RW

PHY Address 1FH

Initial Value 0040H

Bit Position	Bit Name	Function
15-13	(RESERVED)	Reserved (Write 0 and ignore reading)
12	AUTODONE	Completion notice of auto negotiation 0：Incomplete or auto negotiation not set 1：Completion
11-7	(RESERVED)	Reserved (Write 0 and ignore reading)
6	ENABLE_4B5B	Enable/disable settings in 4B/5B encoding/decoding 0：Invalid (Bypass 4B/5B encoding/decoding) 1：Valid
5	(RESERVED)	Reserved (Write 0 and ignore reading)
4-2	SPEED_ INDICATION	Shows the speed 001：10Mbps half-duplex 101：10Mbps duplex 010：100Mbps half-duplex 110：100Mbps duplex
1	RX_DV_J2T	Set the delimiter to identify the beginning and the end of the frame. 0：RX_DV rises by JK delimiter and falls down by TR delimiter. 1：RX_DV rises by JK delimiter and falls down by TR delimiter.
0	SCRAMBLE_ DISABLE	Valid/Invalid settings of data scrambing 0：Valid 1：Invalid

7.5 Ethernet PHY function setting register

This register is used to change the behavior can't be controlled by MII management register of built-in Ethernet PHY without going through the serial management interface.

7.5.1 List of registers

Register Name	Abbreviations	Address
Ethernet PHY operation mode control register	PHYMD	4001 06A0H
Ethernet PHY Power-up status register	PHYPUS	4001 06A4H

7.5.2 Ethernet PHY operation mode control register (PHYMD)

PHYMD set the operating mode of Ethernet PHY. It is a read/write accessible register in 32/16-bit units.

Caution This register can be written only in case of releasing protection by specific sequence using system protects command register (SYSPCMD). Please refer to system protect command register (SYSPCMD) for protection releasing procedure. In addition, the special sequence is not necessary in case of reading the value of this register.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Adress
PHYMD	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P1PHYEN	P1FXMODE	P1ATMDIXEN	P0PHYEN	P0FXMODE	P0ATMDIXEN	4001 06A0H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial Value 0000 003FH

Bit Position	Bit Name	Function
5	P1PHYEN	Valid/Invalid PHY of Port1 0：Valid 1：Invalid（Initial value）
4	P1FXMODE	Valid/Invalid FX mode of Port1(including the input and output terminal control) 0：Valid 1：Invalid（Initial value）
3	P1ATMDIXEN	Valid/Invalid MDIX automatic recognition of Port1 0：Invalid 1：Valid（Initial value）
2	P0PHYEN	Valid/Invalid PHY of Port0 0：Valid 1：Invalid（Initial value）
1	P0FXMODE	Valid/Invalid FX mode of Port0(including the input and output terminal control) 0：Valid 1：Invalid（Initial value）
0	P0ATMDIXEN	Valid/Invalid MDIX automatic recognition of Port0 0：Invalid 1：Valid（Initial value）

7.5.3 Ethernet PHY power-up status register (PHYPUS)

This register is used to confirm the Power-up state of the built-in Ethernet PHY. It can be only read-access in 32-bit units.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PHYPUS	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	P1PWRUPRST	P0PWRUPRST	BASE+06A4H
																																	Initial Value
																																	0000 0000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R	R	

Bit Position	Bit Name	Function
1,0	P1PWRUPRST, P0PWRUPRST	Inform the completion of the power-up of the built-in Ethernet PHY. 1：Power-up and reset 0：Power-up is complete

8. Port function

8.1 Features

- Number of I/O ports: 96
- Can function alternately as the I/O pins of other peripheral functions.
- Input or output can be specified by bit unit.

Caution 1. If a signal from a peripheral function pin that functions alternately as a port pin is switched to port mode by changing the PMCn register setting, a spike might occur, depending on the pin status at that time.
The following general countermeasure for spikes should therefore be implemented by software.

- **Switch the pin function while the peripheral function is stopped.**
- **For pins that function alternately as interrupt signal pins, clear the interrupt request flag, and then cancel masking of the interrupt.**
- **Wait until the output value stabilizes and then switch the mode.**

Caution2. Do not externally input an intermediate voltage to input buffers because these buffers do not implement through-current countermeasures.

8.2 Port configuration

The R-IN32M3-EC incorporates eight ports of 3-state I/O port and four real-time control ports. Input or output mode can be specified for ports in 1-bit units. Each port basically consists of 8 bits, but ports 0 to 3 can also be aligned to enable reading and writing in 32-bit units. The real-time ports (RP00 to RP37) can be used for I/O in synchronization with interrupt signals.

Each port has the registers shown below, each of which is used to set the I/O mode and specify the use of the alternate function of the port. The basic circuit configuration is shown in Figure 8.1.

Register name	Purpose and operation	
	Read	Write
Port registers (Pn, RPm)	Used to read the value of the output latch.	Used to set a value to the output latch.
Port mode registers (PMn, RPMm)	Used to read whether the port is in input or output mode.	Used to set the port to input or output mode.
Port mode control registers (PMCn, RPMCm)	Used to read whether the port is used as a port or as an alternate function pin.	Used to specify whether to use a port as a port or for an alternate function.
Port function control registers (PFCn, RPFCm)	Used to read which alternate function of the port is selected, if the port has more than one alternate function.	Used to specify which alternate function of the port to be selected, if the port has more than one alternate function.
Port function control expansion registers (PFCEn, RPFCEm)	Used to read which alternate function of the port is selected, if the port has more than two alternate functions.	Used to specify which alternate function of the port to be selected in combination with the PFCn register setting, if the port has more than two alternate functions.
Port pin input registers (PINn, RPINm)	Used to read the input level of the port pin.	Cannot be written.

Caution If a port that has multiple alternate functions, including external interrupt input, is set to control mode by using the PMCn register, and if the alternate function is used in input mode, the external interrupt input is also shared.

Remark n = 0 to 7, m = 0 -3

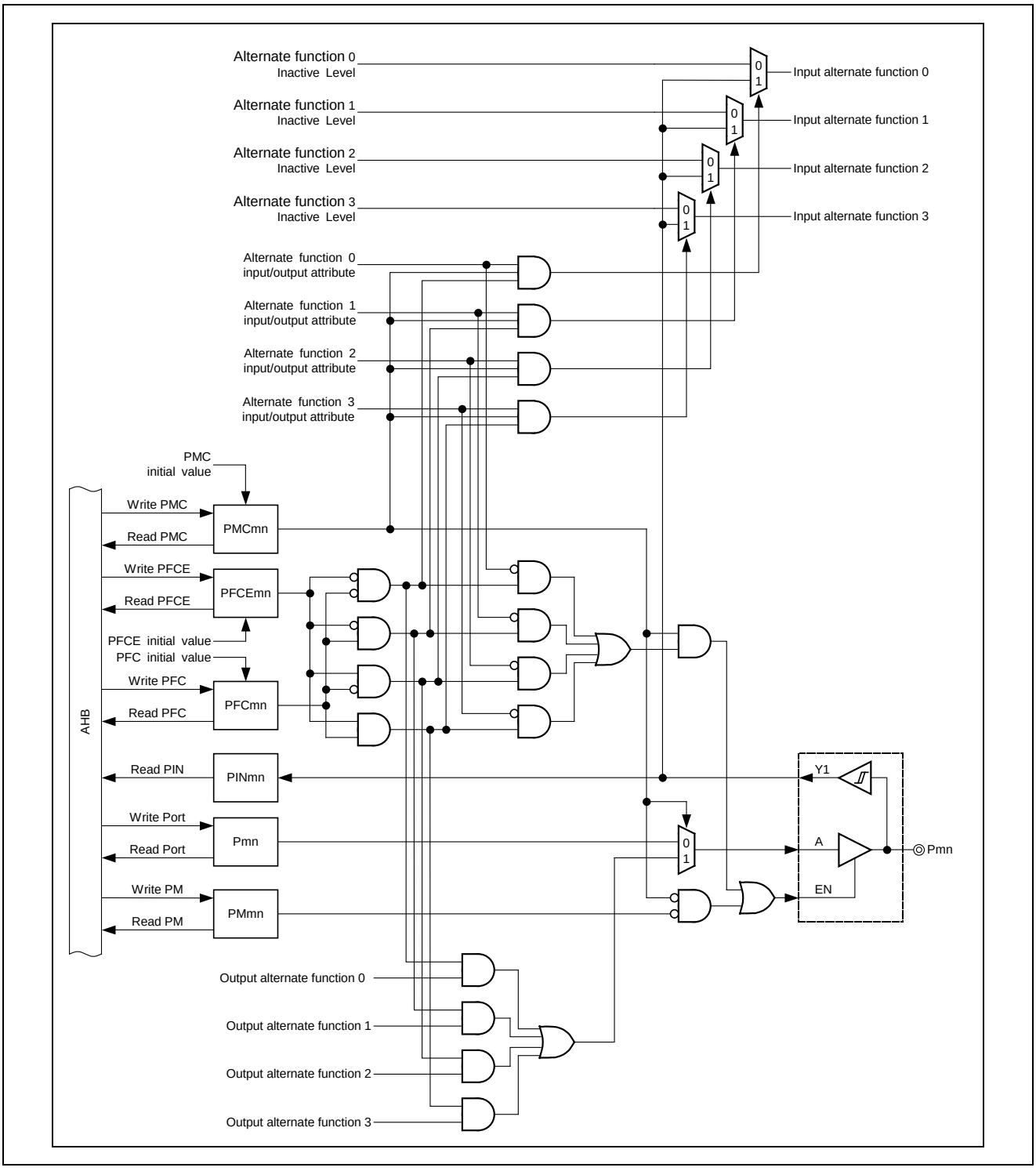


Figure 8.1 Basic port circuit configuration

8.3 Registers

(1/6)

Register name	Symbol	Address
Port register 0 (8 bits)	P0B	400A 3000H
Port register 1 (8 bits)	P1B	400A 3001H
Port register 2 (8 bits)	P2B	400A 3002H
Port register 3 (8 bits)	P3B	400A 3003H
Port register 4 (8 bits)	P4B	400A 3004H
Port register 5 (8 bits)	P5B	400A 3005H
Port register 6 (8 bits)	P6B	400A 3006H
Port register 7 (8 bits)	P7B	400A 3007H
Port register 0 (16 bits)	P0H	400A 3000H
Port register 2 (16 bits)	P2H	400A 3002H
Port register 4 (16 bits)	P4H	400A 3004H
Port register 6 (16 bits)	P8H	400A 3006H
Port register 0 (32 bits)	P0W	400A 3000H
Port register 4 (32 bits)	P4W	400A 3004H
Port mode register 0 (8 bits)	PM0B	400A 3010H
Port mode register 1 (8 bits)	PM1B	400A 3011H
Port mode register 2 (8 bits)	PM2B	400A 3012H
Port mode register 3 (8 bits)	PM3B	400A 3013H
Port mode register 4 (8 bits)	PM4B	400A 3014H
Port mode register 5 (8 bits)	PM5B	400A 3015H
Port mode register 6 (8 bits)	PM6B	400A 3016H
Port mode register 7 (8 bits)	PM7B	400A 3017H
Port mode register 0 (16 bits)	PM0H	400A 3010H
Port mode register 2 (16 bits)	PM2H	400A 3012H
Port mode register 4 (16 bits)	PM4H	400A 3014H
Port mode register 6 (16 bits)	PM6H	400A 3016H
Port mode register 0 (32 bits)	PM0W	400A 3010H
Port mode register 4 (32 bits)	PM4W	400A 3014H

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Register name	Symbol	Address
Port mode control register 0 (8 bits)	PMC0B	400A 3020H
Port mode control register 1 (8 bits)	PMC1B	400A 3021H
Port mode control register 2 (8 bits)	PMC2B	400A 3022H
Port mode control register 3 (8 bits)	PMC3B	400A 3023H
Port mode control register 4 (8 bits)	PMC4B	400A 3024H
Port mode control register 5 (8 bits)	PMC5B	400A 3025H
Port mode control register 6 (8 bits)	PMC6B	400A 3026H
Port mode control register 7 (8 bits)	PMC7B	400A 3027H
Port mode control register 0 (16 bits)	PMC0H	400A 3020H
Port mode control register 2 (16 bits)	PMC2H	400A 3022H
Port mode control register 4 (16 bits)	PMC4H	400A 3024H
Port mode control register 6 (16 bits)	PMC6H	400A 3026H
Port mode control register 0 (32 bits)	PMC0W	400A 3020H
Port mode control register 4 (32 bits)	PMC4W	400A 3024H
Port function control register 0 (8 bits)	PFC0B	400A 3030H
Port function control register 1 (8 bits)	PFC1B	400A 3031H
Port function control register 2 (8 bits)	PFC2B	400A 3032H
Port function control register 3 (8 bits)	PFC3B	400A 3033H
Port function control register 4 (8 bits)	PFC4B	400A 3034H
Port function control register 5 (8 bits)	PFC5B	400A 3035H
Port function control register 6 (8 bits)	PFC6B	400A 3036H
Port function control register 7 (8 bits)	PFC7B	400A 3037H
Port function control register 0 (16 bits)	PFC0H	400A 3030H
Port function control register 2 (16 bits)	PFC2H	400A 3032H
Port function control register 4 (16 bits)	PFC4H	400A 3034H
Port function control register 6 (16 bits)	PFC6H	400A 3036H
Port function control register 0 (32 bits)	PFC0W	400A 3030H
Port function control register 4 (32 bits)	PFC4W	400A 3034H

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Register name	Symbol	Address
Port function control expansion register 0 (8 bits)	PFCE0B	400A 3040H
Port function control expansion register 1 (8 bits)	PFCE1B	400A 3041H
Port function control expansion register 2 (8 bits)	PFCE2B	400A 3042H
Port function control expansion register 3 (8 bits)	PFCE3B	400A 3043H
Port function control expansion register 4 (8 bits)	PFCE4B	400A 3044H
Port function control expansion register 5 (8 bits)	PFCE5B	400A 3045H
Port function control expansion register 6 (8 bits)	PFCE6B	400A 3046H
Port function control expansion register 7 (8 bits)	PFCE7B	400A 3047H
Port function control expansion register 0 (16 bits)	PFCE0H	400A 3040H
Port function control expansion register 2 (16 bits)	PFCE2H	400A 3042H
Port function control expansion register 4 (16 bits)	PFCE4H	400A 3044H
Port function control expansion register 6 (16 bits)	PFCE6H	400A 3046H
Port function control expansion register 0 (32 bits)	PFCE0W	400A 3040H
Port function control expansion register 4 (32 bits)	PFCE4W	400A 3044H
Port pin input register 0 (8 bits)	PIN0B	400A 3050H
Port pin input register 1 (8 bits)	PIN1B	400A 3051H
Port pin input register 2 (8 bits)	PIN2B	400A 3052H
Port pin input register 3 (8 bits)	PIN3B	400A 3053H
Port pin input register 4 (8 bits)	PIN4B	400A 3054H
Port pin input register 5 (8 bits)	PIN5B	400A 3055H
Port pin input register 6 (8 bits)	PIN6B	400A 3056H
Port pin input register 7 (8 bits)	PIN7B	400A 3057H
Port pin input register 0 (16 bits)	PIN0H	400A 3050H
Port pin input register 2 (16 bits)	PIN2H	400A 3052H
Port pin input register 4 (16 bits)	PIN4H	400A 3054H
Port pin input register 6 (16 bits)	PIN6H	400A 3056H
Port pin input register 0 (32 bits)	PIN0W	400A 3050H
Port pin input register 4 (32 bits)	PIN4W	400A 3054H

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Register name	Symbol	Address
RT port register 0 (8 bits)	RP0B	400A 3400H
RT port register 1 (8 bits)	RP1B	400A 3401H
RT port register 2 (8 bits)	RP2B	400A 3402H
RT port register 3 (8 bits)	RP3B	400A 3403H
RT port register 0 (16 bits)	RP0H	400A 3400H
RT port register 2 (16 bits)	RP2H	400A 3402H
RT port register 0 (32 bits)	RP0W	400A 3400H
RT port mode register 0 (8 bits)	RPM0B	400A 3410H
RT port mode register 1 (8 bits)	RPM1B	400A 3411H
RT port mode register 2 (8 bits)	RPM2B	400A 3412H
RT port mode register 3 (8 bits)	RPM3B	400A 3413H
RT port mode register 0 (16 bits)	RPM0H	400A 3410H
RT port mode register 2 (16 bits)	RPM2H	400A 3412H
RT port mode register 0 (32 bits)	RPM0W	400A 3410H
RT port mode control register 0 (8 bits)	RPMC0B	400A 3420H
RT port mode control register 1 (8 bits)	RPMC1B	400A 3421H
RT port mode control register 2 (8 bits)	RPMC2B	400A 3422H
RT port mode control register 3 (8 bits)	RPMC3B	400A 3423H
RT port mode control register 0 (16 bits)	RPMC0H	400A 3420H
RT port mode control register 2 (16 bits)	RPMC2H	400A 3422H
RT port mode control register 0 (32 bits)	RPMC0W	400A 3420H
RT port function control register 0 (8 bits)	RPFC0B	400A 3430H
RT port function control register 1 (8 bits)	RPFC1B	400A 3431H
RT port function control register 2 (8 bits)	RPFC2B	400A 3432H
RT port function control register 3 (8 bits)	RPFC3B	400A 3433H
RT port function control register 0 (16 bits)	RPFC0H	400A 3430H
RT port function control register 2 (16 bits)	RPFC2H	400A 3432H
RT port function control register 0 (32 bits)	RPFC0W	400A 3430H

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Register name	Symbol	Address
RT port function control expansion register 0 (8 bits)	RPFCE0B	400A 3440H
RT port function control expansion register 1 (8 bits)	RPFCE1B	400A 3441H
RT port function control expansion register 2 (8 bits)	RPFCE2B	400A 3442H
RT port function control expansion register 3 (8 bits)	RPFCE3B	400A 3443H
RT port function control expansion register 0 (16 bits)	RPFCE0H	400A 3440H
RT port function control expansion register 2 (16 bits)	RPFCE2H	400A 3442H
RT port function control expansion register 0 (32 bits)	RPFCE0W	400A 3440H
RT port pin input register 0 (8 bits)	RPIN0B	400A 3450H
RT port pin input register 1 (8 bits)	RPIN1B	400A 3451H
RT port pin input register 2 (8 bits)	RPIN2B	400A 3452H
RT port pin input register 3 (8 bits)	RPIN3B	400A 3453H
RT port pin input register 0 (16 bits)	RPIN0H	400A 3450H
RT port pin input register 2 (16 bits)	RPIN2H	400A 3452H
RT port pin input register 0 (32 bits)	RPIN0W	400A 3450H

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Register name	Symbol	Address
Buffer function change register P1L	DRCTLP1L	4001 0228H
Buffer function change register P1H	DRCTLP1H	4001 022CH
Buffer function change register P3L	DRCTLP3L	4001 0238H
Buffer function change register P3H	DRCTLP3H	4001 023CH
Buffer function change register P4L	DRCTLP4L	4001 0240H
Buffer function change register P4H	DRCTLP4H	4001 0244H
Buffer function change register P5L	DRCTLP5L	4001 0248H
Buffer function change register P5H	DRCTLP5H	4001 024CH
Buffer function change register P7H	DRCTLP7H	4001 025CH
Buffer function change register RP0L	DRCTLRP0L	4001 0260H
Buffer function change register RP0H	DRCTLRP0H	4001 0264H
Buffer function change register RP1L	DRCTLRP1L	4001 0268H
Buffer function change register RP1H	DRCTLRP1H	4001 026CH
Buffer function change register RP2L	DRCTLRP2L	4001 0270H
Buffer function change register RP2H	DRCTLRP2H	4001 0274H
Buffer function change register RP3L	DRCTLRP3L	4001 0278H
Buffer function change register RP3H	DRCTLRP3H	4001 027CH

8.3.1 Port registers (P, RP)

The R-IN32M3-EC incorporates twelve 3-state I/O ports. Input or output mode can be specified in 1-bit units. For output ports, the port register can be used to write the output level. If a port register is read, the value of the output latch is read. Use the PINn or RPINm register to read the pin level.

	7	6	5	4	3	2	1	0	Address	Initial value
P0B	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H	00H
P1B	P17	P16	P15	P14	P13	P12	P11	P10	400A 3001H	00H
P2B	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H	00H
P3B	P37	P36	P35	P34	P33	P32	P31	P30	400A 3003H	00H
P4B	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H	00H
P5B	P57	P56	P55	P54	P53	P52	P51	P50	400A 3005H	00H
P6B	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H	00H
P7B	P77	P76	P75	P74	P73	P72	P71	P70	400A 3007H	00H
RP0B	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H	00H
RP1B	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	400A 3401H	00H
RP2B	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H	00H
RP3B	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	400A 3403H	00H

Bit position	Bit name	Function
7 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.2 Port registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P0H	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P2H	P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	400A 3002H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P4H	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P6H	P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	400A 3006H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP0H	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP2H	RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	400A 3402H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

Bit position	Bit name	Function
15 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.3 Port registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

P0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P37	P36	P35	P34	P33	P32	P31	P30	P27	P26	P25	P24	P23	P22	P21	P20	P17	P16	P15	P14	P13	P12	P11	P10	P07	P06	P05	P04	P03	P02	P01	P00	400A 3000H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

P4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
P77	P76	P75	P74	P73	P72	P71	P70	P67	P66	P65	P64	P63	P62	P61	P60	P57	P56	P55	P54	P53	P52	P51	P50	P47	P46	P45	P44	P43	P42	P41	P40	400A 3004H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

RP0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RP37	RP36	RP35	RP34	RP33	RP32	RP31	RP30	RP27	RP26	RP25	RP24	RP23	RP22	RP21	RP20	RP17	RP16	RP15	RP14	RP13	RP12	RP11	RP10	RP07	RP06	RP05	RP04	RP03	RP02	RP01	RP00	400A 3400H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																0000 0000H

Bit position	Bit name	Function
31 to 0	Pmn/RPln	Set the value of the output latch when the port is used in output mode. If read, the value of the output latch is read.

Figure 8.4 Port registers (in 32-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.2 Port mode registers (PM, RPM)

These registers are used to set a port to input or output mode.

	7	6	5	4	3	2	1	0	Address	Initial value
PM0B	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H	FFH
PM1B	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	400A 3011H	FFH
PM2B	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H	FFH
PM3B	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	400A 3013H	FFH
PM4B	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H	FFH
PM5B	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	400A 3015H	FFH
PM6B	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H	FFH
PM7B	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	400A 3017H	FFH
RPM0B	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H	FFH
RPM1B	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	400A 3411H	FFH
RPM2B	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H	FFH
RPM3B	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	400A 3413H	FFH

Bit position	Bit name	Function
7 to 0	PMmn/ RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.5 Port mode registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM0H	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM2H	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	400A 3012H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM4H	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM6H	PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	400A 3016H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM0H	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM2H	RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	400A 3412H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value FFFFH

Bit position	Bit name	Function
15 to 0	PMmn/ RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.6 Port mode registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30	PM27	PM26	PM25	PM24	PM23	PM22	PM21	PM20	PM17	PM16	PM15	PM14	PM13	PM12	PM11	PM10	PM07	PM06	PM05	PM04	PM03	PM02	PM01	PM00	400A 3010H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

PM4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PM77	PM76	PM75	PM74	PM73	PM72	PM71	PM70	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60	PM57	PM56	PM55	PM54	PM53	PM52	PM51	PM50	PM47	PM46	PM45	PM44	PM43	PM42	PM41	PM40	400A 3014H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

RPM0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPM37	RPM36	RPM35	RPM34	RPM33	RPM32	RPM31	RPM30	RPM27	RPM26	RPM25	RPM24	RPM23	RPM22	RPM21	RPM20	RPM17	RPM16	RPM15	RPM14	RPM13	RPM12	RPM11	RPM10	RPM07	RPM06	RPM05	RPM04	RPM03	RPM02	RPM01	RPM00	400A 3410H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: FFFF FFFFH

Bit position	Bit name	Function
31 to 0	PMmn/RPMln	Set the port to input or output mode. 0: Output mode (output buffer is on) 1: Input mode (output buffer is off) (initial value)

Figure 8.7 Port mode registers (in 32-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.3 Port mode control register (PMC, RPMC)

These registers are used to select whether to use a port as a port or for its alternate function.

	7	6	5	4	3	2	1	0	Address	Initial value
PMC0B	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H	00H
PMC1B	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	400A 3021H	00H Note
PMC2B	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	400A 3022H	00H Note
PMC3B	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	400A 3023H	00H Note
PMC4B	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H	00H Note
PMC5B	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	400A 3025H	00H Note
PMC6B	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	400A 3026H	00H Note
PMC7B	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	400A 3027H	00H
RPMC0B	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H	00H Note
RPMC1B	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	400A 3421H	00H Note
RPMC2B	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	400A 3422H	00H Note
RPMC3B	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	400A 3423H	00H Note

Bit position	Bit name	Function
7 to 0	PMCmn/ RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 8.8 Port mode control registers (in 8-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PMC0H	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	Address: 400A 3020H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]
PMC2H	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	Address: 400A 3022H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]
PMC4H	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	Address: 400A 3024H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]
PMC6H	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	Address: 400A 3026H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]
RPMC0H	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	Address: 400A 3420H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]
RPMC2H	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	Address: 400A 3422H
	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value: 0000H[Note]

Bit position	Bit name	Function
15 to 0	PMCmn/ RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 8.9 Port mode control registers (in 16-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC0W	PMC37	PMC36	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30	PMC27	PMC26	PMC25	PMC24	PMC23	PMC22	PMC21	PMC20	PMC17	PMC16	PMC15	PMC14	PMC13	PMC12	PMC11	PMC10	PMC07	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00	400A 3020H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																	0000 0000H[Note]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PMC4W	PMC77	PMC76	PMC75	PMC74	PMC73	PMC72	PMC71	PMC70	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60	PMC57	PMC56	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50	PMC47	PMC46	PMC45	PMC44	PMC43	PMC42	PMC41	PMC40	400A 3024H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																	0000 0000H[Note]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPMC0W	RPMC37	RPMC36	RPMC35	RPMC34	RPMC33	RPMC32	RPMC31	RPMC30	RPMC27	RPMC26	RPMC25	RPMC24	RPMC23	RPMC22	RPMC21	RPMC20	RPMC17	RPMC16	RPMC15	RPMC14	RPMC13	RPMC12	RPMC11	RPMC10	RPMC07	RPMC06	RPMC05	RPMC04	RPMC03	RPMC02	RPMC01	RPMC00	400A 3420H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value
																																	0000 0000H[Note]

Bit position	Bit name	Function
31 to 0	PMCmn/RPMCln	Specify whether to use the port as a port or for its alternate function. 0: Port mode. (The Inactive level is input to the input pin of the alternate function.) 1: Alternate function (control mode)

Figure 8.10 Port mode control registers (in 32-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.4 Port function control registers (PFC, RPFC)

These registers are used to specify which alternate function is used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFC0B	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H	00H
PFC1B	0	0	0	0	0	PFC12	PFC11	PFC10	400A 3031H	00H
PFC2B	PFC27	PFC26	0	PFC24	PFC23	PFC22	0	0	400A 3032H	00H Note1
PFC3B	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	400A 3033H	00H Note1
PFC4B	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H	00H Note1
PFC5B	PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	400A 3035H	00H Note1
PFC6B	0	0	0	0	0	0	0	0	400A 3036H	00H Note1
PFC7B	PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	400A 3037H	00H
RPFC0B	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H	00H
RPFC1B	0	0	0	0	0	0	0	0	400A 3431H	00H
RPFC2B	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H	00H
RPFC3B	0	0	0	0	0	0	0	0	400A 3433H	00H

Bit position	Bit name	Function
7 to 0	PFCmn/ RPFCmn	Specify whether to use alternate functions 1 and 3 or alternate functions 2 and 4. 0: Alternate function 1 Note 2/Alternate function 3 Note 3 1: Alternate function 2 Note 2/Alternate function 4 Note 3

Figure 8.11 Port function control registers (in 8-bit notation)

Note1. The initial value depends on the pin status. For details, see 2.2 Port status.

Note2. To use alternate function 1 or 2, the bit corresponding to the function in the PFCE/RPFCE register must be set to 0.

Note3. To use alternate function 3 or 4, the bit corresponding to the function in the PFCE/RPFCE register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC0H	0	0	0	0	0	PFC12	PFC11	PFC10	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H
	0	0	0	0	0	R/W	R/W	R/W	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC2H	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	PFC25	PFC24	PFC23	PFC22	0	0	400A 3032H
	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC4H	PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
	R/W	R/W	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC6H	PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	0	0	0	0	0	0	0	0	400A 3036H
	R/W	R/W	0	R/W	R/W	R/W	0	R/W	0	0	0	0	0	0	0	0	Initial value 0000H[Note 1]

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC0H	0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H
	0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	0	R/W	R/W	R/W	Initial value 0000H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC2H	0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	400A 3432H
	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	Initial value 0000H

Bit position	Bit name	Function
15 to 0	PFCmn/ RPFCln	Specify whether to use alternate function 1 or 2. 0: Alternate function 1/Alternate function 3 1: Alternate function 2/Alternate function 4

Figure 8.12 Port function control registers (in 16-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC0W	PFC37	PFC36	PFC35	PFC34	PFC33	PFC32	0	0	PFC27	PFC26	0	PFC24	PFC23	PFC22	0	0	0	0	0	0	0	PFC12	PFC11	PFC10	1	PFC06	PFC05	PFC04	PFC03	PFC02	PFC01	PFC00	400A 3030H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	0	R/W	R/W	R/W	0	0	0	0	0	0	0	R/W	R/W	R/W	1	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 0000H[Note]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFC4W	PFC77	PFC76	0	PFC74	PFC73	PFC72	0	PFC70	0	0	0	0	0	0	0	0	PFC57	PFC56	0	PFC54	PFC53	PFC52	0	0	PFC47	PFC46	PFC45	PFC44	PFC43	PFC42	PFC41	PFC40	400A 3034H
R/W	R/W	R/W	0	R/W	R/W	R/W	0	R/W	0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 0000H[Note]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFC0W	0	0	0	0	0	0	0	0	RPFC27	RPFC26	RPFC25	RPFC24	0	0	0	RPFC20	0	0	0	0	0	0	0	0	RPFC07	RPFC06	0	RPFC04	0	RPFC02	RPFC01	RPFC00	400A 3430H
R/W	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	0	0	0	R/W	0	0	0	0	0	0	0	0	R/W	R/W	0	R/W	0	R/W	R/W	R/W	Initial value 0000 0000H[Note]

Bit position	Bit name	Function
31 to 0	PFCmn/RPFCln	Specify whether to use alternate function 1 or 2. 0: Alternate function 1/Alternate function 3 1: Alternate function 2/Alternate function 4

Figure 8.13 Port function control registers (in 32-bit notation)

Note The initial value depends on the pin status. For details, see 2.2 Port status.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.5 Port function control expansion registers (PFCE, RPFCE)

These registers are used to specify which alternate expansion function is used. These registers can be set in 1-bit units.

	7	6	5	4	3	2	1	0	Address	Initial value
PFCE0B	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0	400A 3040H	00H
PFCE1B	0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	400A 3041H	00H
PFCE2B	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H	00H
PFCE3B	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	400A 3043H	00H Note 1
PFCE4B	0	0	0	0	0	PFCE42	0	0	400A 3044H	00H Note 1
PFCE5B	0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	400A 3045H	00H Note 1
PFCE6B	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H	00H Note 1
PFCE7B	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	400A 3047H	00H
RPFCE0B	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H	00H Note 1
RPFCE1B	0	0	0	0	0	0	0	0	400A 3441H	00H Note 1
RPFCE2B	0	0	0	0	0	0	0	0	400A 3442H	00H Note 1
RPFCE3B	0	0	0	0	0	0	0	0	400A 3443H	00H Note 1

Bit position	Bit name	Function
7 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1 Note 2/Alternate function 2 Note 3 1: Alternate function 3 Note 2/Alternate function 4 Note 3

Figure 8.14 Port function control expansion registers (in 8-bit notation)

Note1. The initial value depends on the pin status. For details, see 2.2 Port status.

Note2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

Note3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PFCE0H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0	400A 3040H
0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000H

PFCE2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	400A 3042H
R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H[Note 1]

PFCE4H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0	400A 3044H
0	0	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0	Initial value 0000H[Note 1]

PFCE6H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	400A 3046H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	0	0	Initial value 0000H[Note 1]

RPFCE0H[2]

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000H[Note 1]

RPFCE2H

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	400A 3442H
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Initial value 0000H[Note 1]

Bit position	Bit name	Function
15 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1[Note 2]/Alternate function 2[Note 3] 1: Alternate function 3[Note 2]/Alternate function 4[Note 3]

Figure 8.15 Port function control expansion registers (in 16-bit notation)

Note1. The initial value depends on the pin status. For details, see 2.2 Port status.

Note2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

Note3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE0W	PFCE37	PFCE36	PFCE35	PFCE34	PFCE33	PFCE32	0	0	0	PFCE26	PFCE25	PFCE24	PFCE23	PFCE22	PFCE21	PFCE20	0	0	0	0	PFCE13	PFCE12	PFCE11	PFCE10	PFCE07	PFCE06	PFCE05	PFCE04	PFCE03	PFCE02	0	0	400A 3040H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	Initial value 0000 0000H[Note 1]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PFCE4W	PFCE77	PFCE76	PFCE75	PFCE74	PFCE73	PFCE72	PFCE71	PFCE70	0	0	PFCE65	PFCE64	PFCE63	PFCE62	0	0	0	0	0	PFCE54	PFCE53	PFCE52	PFCE51	PFCE50	0	0	0	0	0	PFCE42	0	0	400A 3044H
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	0	0	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	0	0	0	0	0	R/W	0	0	Initial value 0000 0000H[Note 1]

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPFCE0W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RPFCE05	RPFCE04	RPFCE03	RPFCE02	RPFCE01	RPFCE00	400A 3440H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 0000H[Note 1]

Bit position	Bit name	Function
31 to 0	PFCEmn/ RPFCEln	Specify whether to use alternate functions 1 and 2 or alternate functions 3 and 4. 0: Alternate function 1[Note 2]/Alternate function 2[Note 3] 1: Alternate function 3[Note 2]/Alternate function 4[Note 3]

Figure 8.16 Port function control expansion registers (in 32-bit notation)

Note1. The initial value depends on the pin status. For details, see 2.2 Port status.

Note2. To use alternate function 1 or 3, the bit corresponding to the function in the PFC/RPFC register must be set to 0.

Note3. To use alternate function 2 or 4, the bit corresponding to the function in the PFC/RPFC register must be set to 1.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.3.6 Port pin input registers (PIN, RPIN)

These are read-only registers for reading the input level of port pins.

	7	6	5	4	3	2	1	0	Address	Initial value
PIN0B	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H	Undefined
PIN1B	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	400A 3051H	Undefined
PIN2B	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	400A 3052H	Undefined
PIN3B	PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	400A 3053H	Undefined
PIN4B	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H	Undefined
PIN5B	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	400A 3055H	Undefined
PIN6B	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	400A 3056H	Undefined
PIN7B	PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	400A 3057H	Undefined
RPIN0B	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H	Undefined
RPIN1B	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	400A 3451H	Undefined
RPIN2B	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	400A 3452H	Undefined
RPIN3B	RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	400A 3453H	Undefined

Bit position	Bit name	Function
7 to 0	PINmn/ RPINln	Use to read the input level of the port pin.

Figure 8.17 Port pin input registers (in 8-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN0H	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13	PIN 12	PIN 11	PIN 10	PIN 07	PIN 06	PIN 05	PIN 04	PIN 03	PIN 02	PIN 01	PIN 00	Address: 400A 3050H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN2H	PIN 37	PIN 36	PIN 35	PIN 34	PIN 33	PIN 32	PIN 31	PIN 30	PIN 27	PIN 26	PIN 25	PIN 24	PIN 23	PIN 22	PIN 21	PIN 20	Address: 400A 3052H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN4H	PIN 57	PIN 56	PIN 55	PIN 54	PIN 53	PIN 52	PIN 51	PIN 50	PIN 47	PIN 46	PIN 45	PIN 44	PIN 43	PIN 42	PIN 41	PIN 40	Address: 400A 3054H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PIN6H	PIN 77	PIN 76	PIN 75	PIN 74	PIN 73	PIN 72	PIN 71	PIN 70	PIN 67	PIN 66	PIN 65	PIN 64	PIN 63	PIN 62	PIN 61	PIN 60	Address: 400A 3056H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RPIN0H	RPIN 17	RPIN 16	RPIN 15	RPIN 14	RPIN 13	RPIN 12	RPIN 11	RPIN 10	RPIN 07	RPIN 06	RPIN 05	RPIN 04	RPIN 03	RPIN 02	RPIN 01	RPIN0 0	Address: 400A 3450H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
RPIN2H	RPIN 37	RPIN 36	RPIN 35	RPIN 34	RPIN 33	RPIN 32	RPIN 31	RPIN 30	RPIN 27	RPIN 26	RPIN 25	RPIN 24	RPIN 23	RPIN 22	RPIN 21	RPIN2 0	Address: 400A 3452H
	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value: Undefined

Bit position	Bit name	Function
15 to 0	PINmn/ RPINln	Use to read the input level of the port pin.

Figure 8.18 Port pin input registers (in 16-bit notation)

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

PIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN37	PIN36	PIN35	PIN34	PIN33	PIN32	PIN31	PIN30	PIN27	PIN26	PIN25	PIN24	PIN23	PIN22	PIN21	PIN20	PIN17	PIN16	PIN15	PIN14	PIN13	PIN12	PIN11	PIN10	PIN07	PIN06	PIN05	PIN04	PIN03	PIN02	PIN01	PIN00	400A 3050H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
R/W																																Undefined

PIN4W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
PIN77	PIN76	PIN75	PIN74	PIN73	PIN72	PIN71	PIN70	PIN67	PIN66	PIN65	PIN64	PIN63	PIN62	PIN61	PIN60	PIN57	PIN56	PIN55	PIN54	PIN53	PIN52	PIN51	PIN50	PIN47	PIN46	PIN45	PIN44	PIN43	PIN42	PIN41	PIN40	400A 3054H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
R/W																																Undefined

RPIN0W

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
RPIN37	RPIN36	RPIN35	RPIN34	RPIN33	RPIN32	RPIN31	RPIN30	RPIN27	RPIN26	RPIN25	RPIN24	RPIN23	RPIN22	RPIN21	RPIN20	RPIN17	RPIN16	RPIN15	RPIN14	RPIN13	RPIN12	RPIN11	RPIN10	RPIN07	RPIN06	RPIN05	RPIN04	RPIN03	RPIN02	RPIN01	RPIN00	400A 3450H
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	Initial value
R/W																																Undefined

Bit position	Bit name	Function
31 to 0	PINmn/RPINln	Use to read the input level of the port pin.

Remark l = 0 to 3, m = 0 to 7, n = 0 to 7

8.4 Available combinations of alternate functions

The combinations of alternate functions that can be specified by using the port-related registers are shown below.

(1) Ports (P00 to P77)

(1/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P00	P00 (output mode)	P00 (input mode)	INTPZ0	CATLEDRUN	-	-
P01	P01 (output mode)	P01 (input mode)	INTPZ1	CATIRQ	-	-
P02	P02 (output mode)	P02 (input mode)	INTPZ2	CATLEDSTER	-	-
P03	P03 (output mode)	P03 (input mode)	INTPZ3	CATLEDERR	-	CCS_MON5
P04	P04 (output mode)	P04 (input mode)	INTPZ4	CATLINKACT0	-	CCS_MON6
P05	P05 (output mode)	P05 (input mode)	INTPZ5	CATLINKACT1	-	CCS_MON7
P06	P06 (output mode)	P06 (input mode)	-	P0LINKLEDZ	-	CCS_MON0
P07	P07 (output mode)	P07 (input mode)	-	P1LINKLEDZ	-	CCS_RESOUT
P10	P10 (output mode)	P10 (input mode)	CATLATCH1	CATSYNC1	-	CCS_REFSTB
P11	P11 (output mode)	P11 (input mode)	CATLATCH0	CATSYNC0	-	CCS_MON4
P12	P12 (output mode)	P12 (input mode)	INTPZ6	-	-	-
P13	P13 (output mode)	P13 (input mode)	INTPZ7	-	CCS_WDTZ / CCM_WDTENZ	-
P14	P14 (output mode)	P14 (input mode)	SMSCK	-	-	-
P15	P15 (output mode)	P15 (input mode)	SMSI	-	-	-
P16	P16 (output mode)	P16 (input mode)	SMSO	-	-	-
P17	P17 (output mode)	P17 (input mode)	SMCSZ	-	-	-
P20	P20 (output mode)	P20 (input mode)	RXD0	–	CCM_LINKERRZ	-
P21	P21 (output mode)	P21 (input mode)	TXD0	–	CCM_ERRZ	-
P22	P22 (output mode)	P22 (input mode)	INTPZ8	CATI2CCLK	CCS_IOTENSU	-
P23	P23 (output mode)	P23 (input mode)	INTPZ9	CATI2CDATA	CCS_SENYU0	-
P24	P24 (output mode)	P24 (input mode)	INTPZ10	ETHSWSECOUT	CCS_SENYU1	-
P25	P25 (output mode)	P25 (input mode)	WDTOUTZ	–	CCS_ERRZ	-
P26	P26 (output mode)	P26 (input mode)	TIN1	TOUT1	CCM_RUNZ / CCS_RUNZ	-
P27	P27 (output mode)	P27 (input mode)	TIN0	TOUT0	-	-

Remark m = 0 to 7, n = 0 to 7

(2/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P30	P30 (output mode)	P30 (input mode)	RXD1	-	-	-
P31	P31 (output mode)	P31 (input mode)	TXD1	-	-	-
P32	P32 (output mode)	P32 (input mode)	DMAREQZ1	-	-	CCS_MON1
P33	P33 (output mode)	P33 (input mode)	DMAACKZ1	-	-	CCS_MON2
P34	P34 (output mode)	P34 (input mode)	DMATCZ1	-	-	CCS_MON3
P35	P35 (output mode)	P35 (input mode)	CSISCK1	INTPZ22	CCM_IRLZ	-
P36	P36 (output mode)	P36 (input mode)	CSISI1	INTPZ23	CCS_FUSEZ	-
P37	P37 (output mode)	P37 (input mode)	CSISO1	INTPZ24	CCM_MSTZ	-
P40	P40 (output mode)	P40 (input mode)	A1	HA1	-	-
P41	P41 (output mode)	P41 (input mode)	WAITZ	HWAITZ	-	-
P42	P42 (output mode)	P42 (input mode)	SLEEPING	HERROUTZ	CCM_SDGCZ	-
P43	P43 (output mode)	P43 (input mode)	INTPZ11	HBUSCLK	-	-
P44	P44 (output mode)	P44 (input mode)	CSZ1	HPGCSZ	-	-
P45	P45 (output mode)	P45 (input mode)	CSISCK0	WAITZ1	-	-
P46	P46 (output mode)	P46 (input mode)	CSISI0	WAITZ2	-	-
P47	P47 (output mode)	P47 (input mode)	CSISO0	WAITZ3	-	-
P50	P50 (output mode)	P50 (input mode)	CSZ3	-	CCM_LNKRUNZ / CCS_LNKRUNZ	-
P51	P51 (output mode)	P51 (input mode)	CSZ2	-	CCM_RDLEDZ / CCS_RDLEDZ	-
P52	P52 (output mode)	P52 (input mode)	TIN3	TOUT3	CCS_SDGATEON	-
P53	P53 (output mode)	P53 (input mode)	CRXD0	CCS_RD	CCM_RD	-
P54	P54 (output mode)	P54 (input mode)	CTXD0	CCS_SD	CCM_SD	-
P55	P55 (output mode)	P55 (input mode)	CRXD1	–	–	-
P56	P56 (output mode)	P56 (input mode)	CTXD1	CATRESTOUT	-	-
P57	P57 (output mode)	P57 (input mode)	TIN2	TOUT2	-	-

Remark m = 0 to 7, n = 0 to 7

(3/3)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			PFCEmn = 0		PFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	PFCmn = 0	PFCmn = 1	PFCmn = 0	PFCmn = 1
P60	P60 (output mode)	P60 (input mode)	SCL0	–	–	–
P61	P61 (output mode)	P61 (input mode)	SDA0	–	–	–
P62	P62 (output mode)	P62 (input mode)	RTDMAREQZ	–	CCM_MDIN0	–
P63	P63 (output mode)	P63 (input mode)	RTDMAACKZ	–	CCM_MDIN1	–
P64	P64 (output mode)	P64 (input mode)	RTDMATCZ	–	CCM_MDIN2	–
P65	P65 (output mode)	P65 (input mode)	DMAREQZ0	–	CCM_MDIN3	–
P66	P66 (output mode)	P66 (input mode)	DMAACKZ0	–	–	–
P67	P67 (output mode)	P67 (input mode)	DMATCZ0	–	–	–
P70	P70 (output mode)	P70 (input mode)	CSICS00	P0DUPLEXLEDZ	CCS_STATION_NO_0 / CCM_SNIN0	–
P71	P71 (output mode)	P71 (input mode)	CSICS01	-	CCS_STATION_NO_1 / CCM_SNIN1	–
P72	P72 (output mode)	P72 (input mode)	CSICS10	P0SPEED100LEDZ	CCS_STATION_NO_2 / CCM_SNIN2	–
P73	P73 (output mode)	P73 (input mode)	CSICS11	P0SPEED10LEDZ	CCS_STATION_NO_3 / CCM_SNIN3	–
P74	P74 (output mode)	P74 (input mode)	INTPZ12	P1DUPLEXLEDZ	CCS_STATION_NO_4 / CCM_SNIN4	–
P75	P75 (output mode)	P75 (input mode)	INTPZ13	-	CCS_STATION_NO_5 / CCM_SNIN5	–
P76	P76 (output mode)	P76 (input mode)	INTPZ14	P1SPEED100LEDZ	CCS_STATION_NO_6 / CCM_SNIN6	–
P77	P77 (output mode)	P77 (input mode)	INTPZ15	P1SPEED10LEDZ	CCS_STATION_NO_7 / CCM_SNIN7	–

Remark m = 0 to 7, n = 0 to 7

(2) Real-time control ports (RP00 to RP37)

Pin name	PMCmn = 0 (port mode)		PMCmn = 1 (control mode)			
			RPFCEmn = 0		RPFCEmn = 1	
	PMmn = 0 (output port)	PMmn = 1 (input port)	RPFCmn = 0	RPFCmn = 1	RPFCmn = 0	RPFCmn = 1
RP00	RP00 (output mode)	RP00 (input mode)	INTPZ16	SCL1	CCM_SDLEDZ / CCS_SDLEDZ	-
RP01	RP01 (output mode)	RP01 (input mode)	INTPZ17	SDA1	CCM_SMSTZ	-
RP02	RP02 (output mode)	RP02 (input mode)	INTPZ18	P0ACTLEDZ	CCS_BS1	-
RP03	RP03 (output mode)	RP03 (input mode)	INTPZ19	–	CCS_BS2	-
RP04	RP04 (output mode)	RP04 (input mode)	INTPZ20	P1ACTLEDZ	CCS_BS4	-
RP05	RP05 (output mode)	RP05 (input mode)	INTPZ21	–	CCS_BS8	-
RP06	RP06 (output mode)	RP06 (input mode)	WRZ2	HWRZ2	-	–
RP07	RP07 (output mode)	RP07 (input mode)	WRZ3	HWRZ3	-	–
RP10	RP10 (output mode)	RP10 (input mode)	D24/HD24	–	-	–
RP11	RP11 (output mode)	RP11 (input mode)	D25/HD25	–	-	–
RP12	RP12 (output mode)	RP12 (input mode)	D26/HD26	–	-	–
RP13	RP13 (output mode)	RP13 (input mode)	D27/HD27	–	-	–
RP14	RP14 (output mode)	RP14 (input mode)	D28/HD28	–	-	–
RP15	RP15 (output mode)	RP15 (input mode)	D29/HD29	–	-	–
RP16	RP16 (output mode)	RP16 (input mode)	D30/HD30	–	-	–
RP17	RP17 (output mode)	RP17 (input mode)	D31/HD31	–	-	-
RP20	RP20 (output mode)	RP20 (input mode)	BCYSTZ	HBCYSTZ	-	-
RP21	RP21 (output mode)	RP21 (input mode)	A21	–	-	-
RP22	RP22 (output mode)	RP22 (input mode)	A22	–	–	-
RP23	RP23 (output mode)	RP23 (input mode)	A23	–	–	-
RP24	RP24 (output mode)	RP24 (input mode)	A24	INTPZ25	–	-
RP25	RP25 (output mode)	RP25 (input mode)	A25	INTPZ26	–	-
RP26	RP26 (output mode)	RP26 (input mode)	A26	INTPZ27	–	-
RP27	RP27 (output mode)	RP27 (input mode)	A27	INTPZ28	–	-
RP30	RP30 (output mode)	RP30 (input mode)	D16/HD16	-	–	-
RP31	RP31 (output mode)	RP31 (input mode)	D17/HD17	-	–	-
RP32	RP32 (output mode)	RP32 (input mode)	D18/HD18	-	–	-
RP33	RP33 (output mode)	RP33 (input mode)	D19/HD19	-	–	-
RP34	RP34 (output mode)	RP34 (input mode)	D20/HD20	-	–	-
RP35	RP35 (output mode)	RP35 (input mode)	D21/HD21	-	–	-
RP36	RP36 (output mode)	RP36 (input mode)	D22/HD22	-	–	-
RP37	RP37 (output mode)	RP37 (input mode)	D23/HD23	-	–	-

Remark m = 0 to 3, n = 0 to 7

8.5 Buffer function change registers (DRCTLP)

For some port pins, the driving capability and whether to connect a pull-up or pull-down resistor can be specified individually.

Set up the DRCTLP registers during initialization after the reset period ends. After that, the setting of each DRCTLP register can only be changed when the corresponding buffer function change pin is not being used. For example, a DRCTLP register setting can be changed at times when only a memory space is being accessed internally.

The DRCTLP register setting becomes valid regardless of the operating mode of the pin (port mode, or control mode in which an alternate function is used).

- Access These registers can be read and written in 32-bit or 16-bit units.

Caution1. These registers are write-protected and can only be written after being protection-unlocked by using a special instruction sequence initiated by using the system protection command register (SYSPCMD). For how to unlock protection, see the description of the system protection command register (SYSPCMD). No special instruction sequence is required for reading these registers.

Caution2. Changing the pull-up/pull-down resistor setting affects the level when a pin enters a high-impedance state.

8.5.1 Port 1 buffer function change registers (DRCTLP1L, DRCTLP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP13	PDIOP13	0	1	PUIOP12	PDIOP12	0	1	PUIOP11	PDIOP11	0	1	PUIOP10	PDIOP10	IOLP101	IOLP100	BASE+0228H
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	R/W	R/W	0000 9959H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP17	PDIOP17	0	1	PUIOP16	PDIOP16	0	1	PUIOP15	PDIOP15	0	1	PUIOP14	PDIOP14	0	1	BASE+022CH
																																	Initial value
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3. 2	PUIOP1n, PDIOP1n	Specify whether to connect a pull-up or pull-down resistor to the P17 to P10 pins.
1, 0	IOLP101, IOLP100	Specify the driving capability of the P10 pin.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P17 to P10 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1:	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of P10 pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.2 Port 3 buffer function change registers (DRCTLP3L, DRCTLP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP33	PDIOP33	0	1	PUIOP32	PDIOP32	0	1	PUIOP31	PDIOP31	0	1	PUIOP30	PDIOP30	0	1	BASE+0238H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP37	PDIOP37	IOLP371	IOLP370	PUIOP36	PDIOP36	0	1	PUIOP35	PDIOP35	0	1	PUIOP34	PDIOP34	0	1	BASE+023CH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP3n, PDIOP3n	Specify whether to connect a pull-up or pull-down resistor to the P37 to P30 pins.
13, 12	IOLP371, IOLP370	Specify the driving capability of the P37 pin.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P37 to P30 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of P37 pin
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.3 Port 4 buffer function change registers (DRCTLP4L, DRCTLP4H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP43	PDIOP43	0	1	PUIOP42	PDIOP42	0	1	PUIOP41	PDIOP41	0	1	PUIOP40	PDIOP40	0	1	BASE+0240H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP4H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP47	PDIOP47	0	1	PUIOP46	PDIOP46	0	1	PUIOP45	PDIOP45	0	1	PUIOP44	PDIOP44	0	1	BASE+0244H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	R/W	R/W	0	1	Initial value 0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP4n, PDIOP4n	Specify whether to connect a pull-up or pull-down resistor to the P47 to P40 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P47 to P40 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

Remark n = 7 to 0

8.5.4 Port 5 buffer function change registers (DRCTLP5L, DRCTLP5H) <R>

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP52	PDIOP52	0	1	PUIOP51	PDIOP51	IOLP511	IOLP510	PUIOP50	PDIOP50	IOLP501	IOLP500	BASE+0248H
																																	Initial value
																																	0000 0599H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLP5H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIOP57	PDIOP57	0	1	0	0	0	0	0	0	0	0	0	0	0	0	BASE+024CH
																																	Initial value
																																	0000 9000H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	0	1	0	0	0	0	0	0	0	0	0	0	0	0	

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIOP5n, PDIOP5n	Specify whether to connect a pull-up or pull-down resistor to the P57 and P52 to P50 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the P57 and P52 to P50 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

5, 4, 1, 0	IOLP5n1, IOLP5n0	Specify the driving capability of the P51 to P50 pins. <R>

IOL1	IOL0	Driving capability of P51 to P50 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.5 Real-time port 0 buffer function change registers (DRCTLRP0L, DRCTLRP0H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP03	PDIORP03	IOLRP031	IOLRP030	PUIORP02	PDIORP02	IOLRP021	IOLRP020	PUIORP01	PDIORP01	IOLRP011	IOLRP010	PUIORP00	PDIORP00	IOLRP001	IOLRP000	BASE+0260H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP0H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP07	PDIORP07	IOLRP071	IOLRP070	PUIORP06	PDIORP06	IOLRP061	IOLRP060	PUIORP05	PDIORP05	IOLRP051	IOLRP050	PUIORP04	PDIORP04	IOLRP041	IOLRP040	BASE+0264H
																																	Initial value
																																	0000 9999H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP0n, PDIORP0n	Specify whether to connect a pull-up or pull-down resistor to the RP07 to RP00 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP0n1, IOLRP0n0	Specify the driving capability of the RP07 to RP00 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP07 to RP00 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP07 to RP00 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.6 Real-time port 1 buffer function change registers (DRCTLRP1L, DRCTLRP1H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP13	PDIORP13	IOLRP131	IOLRP130	PUIORP12	PDIORP12	IOLRP121	IOLRP120	PUIORP11	PDIORP11	IOLRP111	IOLRP110	PUIORP10	PDIORP10	IOLRP101	IOLRP100	BASE+0268H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP1H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP17	PDIORP17	IOLRP171	IOLRP170	PUIORP16	PDIORP16	IOLRP161	IOLRP160	PUIORP15	PDIORP15	IOLRP151	IOLRP150	PUIORP14	PDIORP14	IOLRP141	IOLRP140	BASE+026CH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP1n, PDIORP1n	Specify whether to connect a pull-up or pull-down resistor to the RP17 to RP10 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP1n1, IOLRP1n0	Specify the driving capability of the RP17 to RP10 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP17 to RP10 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP17 to RP10 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.7 Real-time port 2 buffer function change registers (DRCTLRP2L, DRCTLRP2H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP23	PDIORP23	IOLRP231	IOLRP230	PUIORP22	PDIORP22	IOLRP221	IOLRP220	PUIORP21	PDIORP21	IOLRP211	IOLRP210	PUIORP20	PDIORP20	IOLRP201	IOLRP200	BASE+0270H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 5559H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP2H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP27	PDIORP27	IOLRP271	IOLRP270	PUIORP26	PDIORP26	IOLRP261	IOLRP260	PUIORP25	PDIORP25	IOLRP251	IOLRP250	PUIORP24	PDIORP24	IOLRP241	IOLRP240	BASE+0274H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 5555H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP2n, PDIORP2n	Specify whether to connect a pull-up or pull-down resistor to the RP27 to RP20 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP2n1, IOLRP2n0	Specify the driving capability of the RP27 to RP20 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP27 to RP20 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP27 to RP20 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.5.8 Real-time port 3 buffer function change registers (DRCTLRP3L, DRCTLRP3H)

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3L	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP33	PDIORP33	IOLRP331	IOLRP330	PUIORP32	PDIORP32	IOLRP321	IOLRP320	PUIORP31	PDIORP31	IOLRP311	IOLRP310	PUIORP30	PDIORP30	IOLRP301	IOLRP300	BASE+0278H
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Address
DRCTLRP3H	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUIORP37	PDIORP37	IOLRP371	IOLRP370	PUIORP36	PDIORP36	IOLRP361	IOLRP360	PUIORP35	PDIORP35	IOLRP351	IOLRP350	PUIORP34	PDIORP34	IOLRP341	IOLRP340	BASE+027CH
R/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	Initial value 0000 9999H

Bit position	Bit name	Function
31 to 16	–	Reserved. (Be sure to write 0 to these bits. If read, 0 is returned.)
15, 14, 11, 10, 7, 6, 3, 2	PUIORP3n, PDIORP3n	Specify whether to connect a pull-up or pull-down resistor to the RP37 to RP30 pins.
13, 12, 9, 8, 5, 4, 1, 0	IOLRP3n1, IOLRP3n0	Specify the driving capability of the RP37 to RP30 pins.

PUIO	PDIO	Connection of a pull-up or pull-down resistor to the RP37 to RP30 pins
0	0	Do not connect a pull-up or pull-down resistor.
0	1	Connect a pull-down resistor.
1	0	Connect a pull-up resistor.
1	1	Setting prohibited

IOL1	IOL0	Driving capability of RP37 to RP30 pins
0	1	6 mA (recommended)
1	1	12 mA
Other than above		Setting prohibited

Remark n = 7 to 0

8.6 Operation of port functions

The port operation differs depending on the I/O mode setting, as shown below.

8.6.1 Reading and writing via I/O ports

(1) In output mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). The value of the output latch is output from the pin.

The value written to the output latch is held until another value is written.

The value of the output latch (Pn or RPn) can be read by reading port register n (Pn or RPn).

To directly read the pin level, read port pin input register n (PINn or RPINn).

(2) In input mode

If a value is written to port register n (Pn or RPn), the value is written to that port's output latch (Pn or RPn). However, the pin status does not change because the output buffer is off.

The value written to the output latch is held until another value is written.

To read the input level, read port pin input register n (PINn or RPINn).

8.6.2 Alternate function pin output status in control mode

The port pin level can be read directly by reading port pin input register n (PINn or RPINn), regardless of the settings in the PMCn, PMn, PFCn, and PFCEn registers.

8.7 Trigger-synchronous ports (RP00 to RP37)

The status of the 32-bit port pins RP00 to RP37 is updated in synchronization with an interrupt from an on-chip peripheral function.

Use the RPTRGMD register to specify whether to set a port to trigger-synchronous port control mode in 1-bit units. To select the trigger, use the RPTFR0 to RPTFR3 registers.

For details, see R-IN32M3 User's Manual - Peripheral Functions.

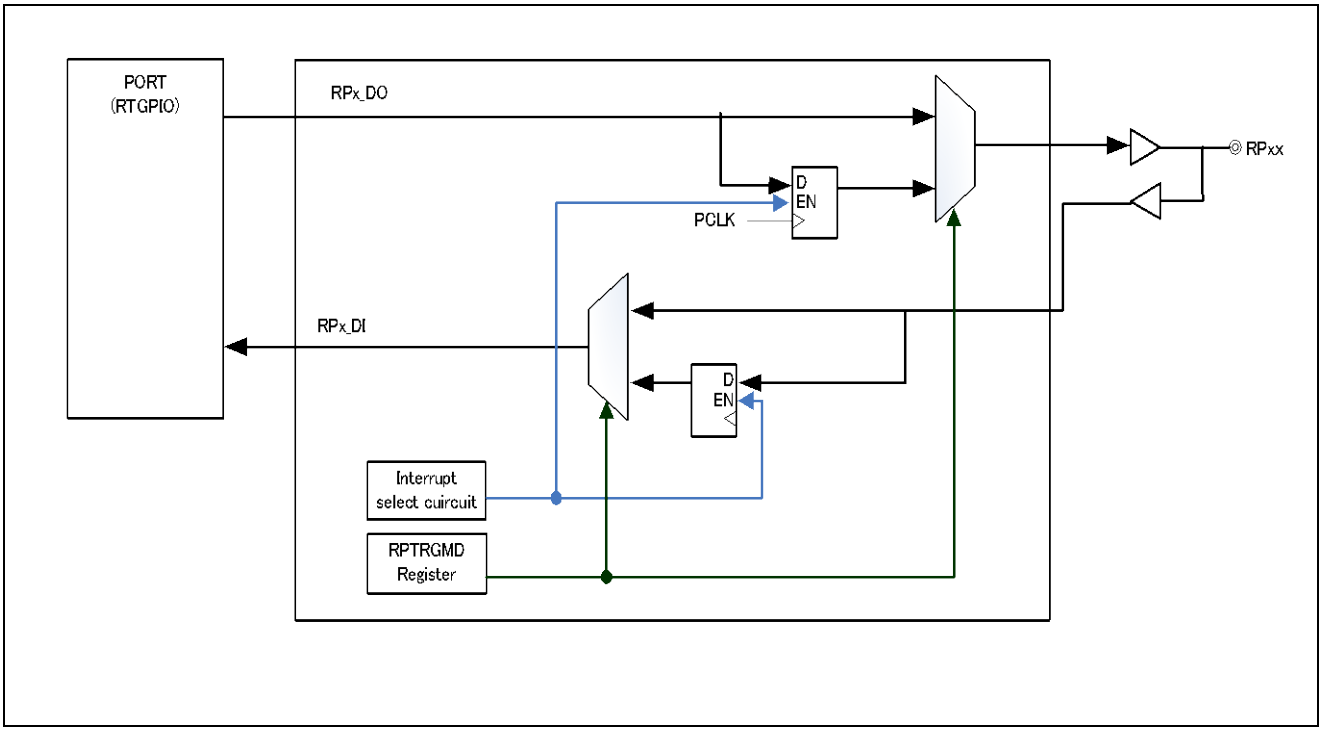

Figure 8.19 Configuration of Trigger-Synchronous Ports

9. Electrical Specifications

Please refer to R-IN32M3 series datasheet for the Electrical Specifications.

REVISION HISTORY	R-IN32M3-EC User's Manual

Rev.	Date	Description	
		Page	Summary
1.00 (Preliminary)	2013.2.8	-	First edition issued
1.00	Apr 03,2013	overall	Modification of English expressions
		overall	Change the description of "CC-Link" "CC-Link (Slave)" → "CC-Link (Remote device station)"
		1	Modification of the contents of ***1.1 Introduction***
		3	Standby mode deletion of Table1.1 Overview of R-IN32M3-EC
		9	Modification of the status of BUSCLK during the reset of ***2.1.2 External Memory Interface Signals*** Addition of synchronous burst access MEMC information of ***2.1.2 External Memory Interface Signals***
		10	Modification of the status of HD0-HD15, HBCYSTZ during the reset of ***2.1.3 External MPU Interface Signals***
		21	Modification of PONRZ function of ***2.1.16 System Signals*** Addition the signals of HOTRESETZ, VDDQ_MII of ***2.1.16 System Signals***
		24	Modification of the status of P40 of ***2.2Port status*** Modification of the contents of Note1 and Note2 of ***2.2Port status***
1.01	Dec 09 ,2013	overall	Modification of the supported station of CC-Link
2.00	Feb 07,2014	4	Addition of a connection of GPIO block and DMAC_RTPORT bus of ***1.3 Internal block diagram*** Addition of a connection of RealTimeGPIO block and DMAC bus of ***1.3 Internal block diagram***
		6-24	Addition the status after reset timing of ***2.1 Signals by function***
		21	Add ***CCM_CLK80M*** pins to list of ***2.1.15 CC-Link Signals (Remote device station)***
		22	Deletion the description about VDDQ_MII of ***2.1.16 System Signals***
		24	Modification of Boot mode select of ***2.1.18 Operation mode Setting Signals***
		25	Addition Synchronous burst MEMC of ***2.2 Port status***
		28-29	Addition of a resister value of Pull up/down of ***2.3.5 Port Signals*** Modification of a description of the drive current of P10/P30/P31/P52 of ***2.3.5 Port Signals***
		29	Modification of title name of ***2.3.7 CC-Link Signal (Intelligent device station, Remote device station)***
		30	Modification of the end address of EtherCAT area of ***Fig.3.1 Memory Map (ALL)***
		33	Modification of the end address of EtherCAT area of ***Fig.3.5 External MPU interface area***
		38	Addition of the contents of Note of INTCCSRFSTB register of ***4.2 Inerruput list***
		41	Adidtion ***6.2 Peripheral circuit of EtherCAT***
		47	Addition ***7.Ether PHY Function***
		96	Modification of initial value of ***Fig.8.7 Port mode registers***

Rev.	Date	Description	
		Page	Summary
2.01	Apr 18,2014	overall	Modification of ***CC-Link Signals (Remote device station)***
		60	Modification of the contents of ACKNOWLEDGEbit of ***7.4.5 Register 5 - Auto-Negotiation Link Partner Ability (Base Page) Register***
3.00	Jun 30,2014	22	Modification of attribution of FB of ***2.1.16 System Signals***
		30	Modification of the end address of EtherCAT area of ***Fig.3.1 Memory Map (ALL)***
		33	Modification of the end address of EtherCAT area of ***Fig.3.5 External MPU interface area***
		40-125	Modification of ***6 EtherCAT Slave Controller function***
3.01	Dec 25,2014	3	Change status for Intelligent device station for CC-Link in ***1.3 Overview***
		196	Remove IOLP521, IOLP520 bit at ***8.5.4 Port 5 buffer function change registers (DRCTLP5L, DRCTLP5H)*** (because driving capability of P52 is fixed to 6mA.)

[Memo]

R-IN32M3 Series User's Manual

R-IN32M3-EC

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